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Electrical characterization of metal-insulator-semiconductor diodes fabricated from laser-ablated $YBa_2Cu_3O_{7-\delta}$ /yttria-stabilized zirconia films on Si substrates

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The purpose of this investigation is to study the electrical properties of the YBCO/YSZ/Si metal-insulator-semiconductor structure and the yttria-stabilized zirconia (YSZ)/Si interface. The YBCO and YSZ layers were epitaxially grown *in situ* on Si by pulsed laser deposition. Current-voltage measurements of devices fabricated on *p*-type Si(100) showed a small leakage current density at 292 K, which decreased further at 80 K. Comparison of capacitance-voltage measurements at 292 K for frequencies between 10 and 400 kHz showed a large variation of capacitance in the accumulation region demonstrating the presence of mobile ions in the YSZ layer. This variation is less pronounced at 80 K. A negative shift of about 5 V in threshold voltage from 292 to 80 K has been attributed to redistribution of charges in the YSZ buffer layer.

The discovery of ceramic materials with superconducting temperatures[1] that overlap the operating temperatures of most silicon devices brought on great efforts to incorporate these materials into silicon technology. In order to deposit epitaxial films of these perovskite-type superconductors on Si, a buffer layer is required.[2] A promising buffer layer is yttria-stabilized zirconia (YSZ), $(Y_2O_3)_{0.09}(ZrO_2)_{0.91}$. It may be grown epitaxially on Si(100) in spite of a -6% lattice mismatch. No deep levels which might affect carrier lifetimes have been found for Zr in Si.[3] YSZ is also an excellent diffusion barrier. $YBa_2Cu_3O_{7-\delta}$ is a well-known high-T_c superconductor and has a $+6\%$ lattice mismatch with YSZ in the commonly observed epitaxial orientation.[4] High-quality films of YSZ and YBCO have been fabricated *in situ* with pulsed laser deposition[5] on a *p*-type Si(100) substrate with a dopant concentration of about 1.5×10^{16} cm^{-3}. Both YSZ and YBCO films are 1500 Å thick. Transmission electron microscopy (TEM) of the YSZ/Si interface reveals a layer of SiO_x approximately 50 Å in thickness.[6] The precise role of this layer is unknown but is probably responsible for the low density of states at the interface. Resistivity measurements for these films yield a critical temperature of 86 K with a transition region of less than 2 K. At 77 K these films typically have a critical current density (J_c) of about 2×10^6 A/cm^2.[5]

The YBCO layer is patterned and etched to produce metal (YBCO)-insulator (YSZ)-semiconductor (Si) diodes. Since direct probing on YBCO results in a contact resistance of a few megaohms, low-resistance ohmic contacts need to be formed for meaningful electrical characterization. Two metals commonly used to make contacts to YBCO are silver and gold.[7] It has been reported that most normal metals other than Ag and Au do not make good electrical contacts to YBCO, due in part to the depletion of oxygen from the YBCO surface.[8] We have therefore employed Au to make contacts to the YBCO electrode. To fabricate these contacts, a kovar stencil mask is used. The kovar sheet is patterned with standard photolithographic techniques. The fabricated mask is placed over the sample in an evaporator. Au is evaporated through the mask at a background pressure of 4×10^{-6} Torr. The YBCO gate and the Au contact diameters are 2 mm and 0.4 mm, respectively. From two-point measurements, total resistance including YBCO and the two contacts at room temperature is less than 200 Ω. This resistance is acceptable for current and capacitance measurements. Gold is also evaporated on the back side of the sample to yield an ohmic contact to the substrate.

Results of room-temperature (292 K) current versus voltage (*I-V*) measurements are shown in Fig. 1. This plot shows the leakage current of the device (<9 nA/cm^2) as the voltage is swept from -3 to 3 V and then from 3 to -3 V. The large current flow at initial bias, and apparent current flow through the device at 0 V is due to transient effects of ions in YSZ during the voltage sweep. This transient current was eliminated by sweeping the voltage from 0 to 3 V and then from 0 to -3 V. Low-temperature (80 K) *I-V* measurements reveal even less leakage (<2 nA/cm^2 between -3 and 3 V). Bulk YSZ is an ionic conductor with conductivity that follows an Arrhenius behavior over a wide temperature range with an activation energy of about 1 eV.[9] Pure ZrO_2 is monoclinic, while the cubic phase is stabilized by adding Y_2O_3. Since Y^{3+} substitutes for Zr^{4+}, every two Y^{3+} ions in the YSZ solid solution must induce a mobile oxygen anion vacancy. The

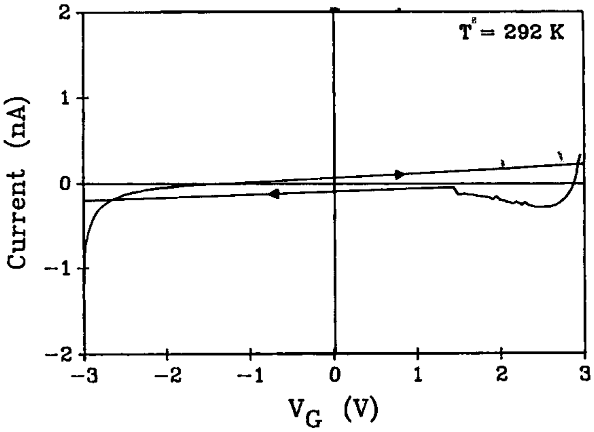

FIG. 1. Room-temperature *I-V* characteristics of a YBCO/YSZ/Si MIS diode swept from − 3 to 3 V and 3 to − 3 V.

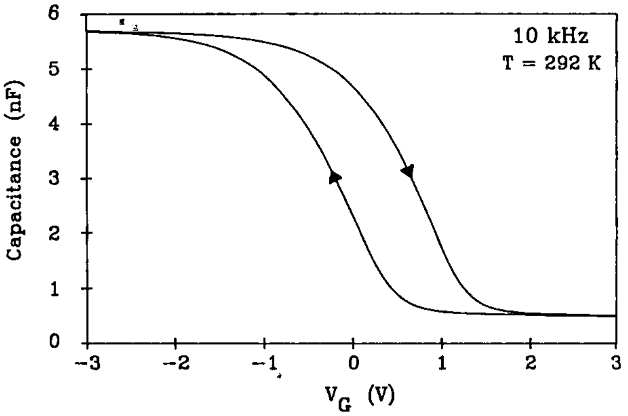

FIG. 3. Room-temperature 10 kHz *C-V* characteristics of a YBCO/YSZ/Si diode swept in the positive and negative gate voltage directions.

resulting conduction by oxygen anions may account in part for the room-temperature leakage and hysteresis, and the decrease thereof at 80 K.

Capacitance versus voltage (*C-V*) measurements at 10, 20, 40, 100, 200, and 400 kHz were performed at 292 K. The gate voltages are swept in the negative direction first and then in the positive direction at a fixed sweep rate and measurement frequency. This procedure helps to restore mobile ions to their original positions so that the true frequency-dependent characteristics can be revealed. As can be seen from Fig. 2, the MIS capacitor shows inversion, depletion, and accumulation regions similar to that of a MOS capacitor. In the accumulation region, there is a decrease in the measured capacitance with increasing frequency. The dielectric constant (K_{ins}) can be estimated from the accumulation capacitance (C_{accum}), assuming that C_{accum} is due to the insulator capacitance only. The dielectric constant of YSZ at 10 kHz is computed to be 31 while that at 400 kHz is 25. This trend of decreasing K_{ins} with increasing frequency is similar to previous reports on bulk YSZ.[10,11] It has been reported[11] that at 200 °C the dielectric constant in bulk YSZ can change by a factor of 2 between 100 Hz and 100 kHz. At room temperature, however, K_{ins} varies only slightly around 30 in the bulk over this frequency range, but is more variable for films, possibly due to defects. In our devices, the C_{accum} decrease with increasing frequency is probably due to anion charge fluctuation in YSZ and in the SiO_x interfacial layer, as well as to K_{ins} variation. In the depletion region, the capacitance curves show a shift in the negative voltage direction with increasing frequency. This behavior is a result of the decrease in C_{accum} with increasing frequency. A comparison of both voltage sweep directions at a single frequency (Fig. 3) reveals considerable hysteresis. This is characteristic of MIS structures with ionic conduction in the dielectric.[12] Hysteresis has also been reported in other MIS structures utilizing YSZ.[13]

C-V measurements were also performed at 80 K, close to the critical temperature of the YBCO film. A dramatic change in the *C-V* characteristics is the negative shift of about 5 V in threshold voltage (Fig. 4). By neglecting interface traps, the flatband voltage V_{fb} is given by[14]

$$V_{fb}=\phi_{ms}-Q_i/C_i, \tag{1}$$

where ϕ_{ms} is the metal-semiconductor work function difference which is presumed temperature independent, C_i is the insulator capacitance, and Q_i is the effective interface charge which is related to the first moment of the insulator charge distribution ρ_i by

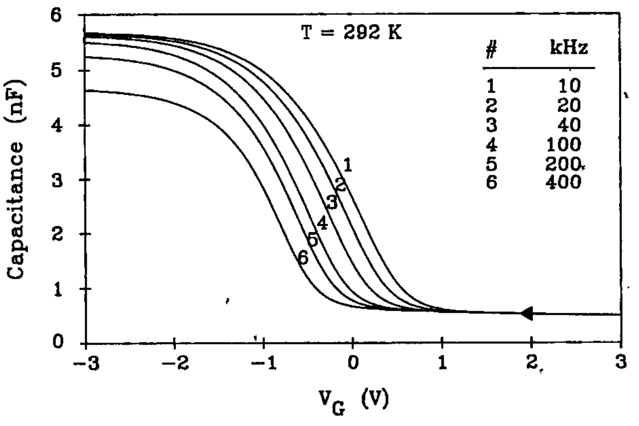

FIG. 2. Room-temperature *C-V* characteristics of a YBCO/YSZ/Si diode swept in the negative gate voltage direction at frequencies between 10 and 400 kHz.

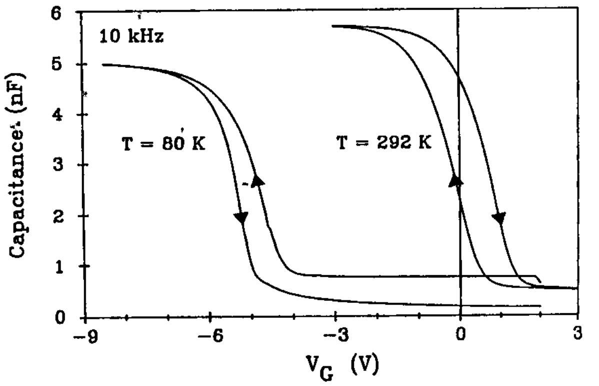

FIG. 4. Comparison of room- and superconducting-temperature 10 kHz *C-V* characteristics of a MIS diode swept in both gate voltage directions. A 5 V shift in the negative direction is observed from room to superconducting temperature.

$$Q_i = \frac{1}{t} \int_0^t \rho_i(x) x \, dx, \tag{2}$$

where t is the insulator thickness. The germane feature is that Q_i is sensitive to the *distribution* of charges in the insulator. The 5 V shift corresponds to a 5×10^{12} cm^{-2} decrease in effective negative charge. We suggest that this decrease is due to a difference between room- and low-temperature insulator charge distributions as a result of the immobilization of oxygen anions within the YSZ layer. Preliminary measurements on devices cooled down under different bias conditions yield changes in the low-temperature threshold voltage, suggesting a memory effect whereby the charge distribution in YSZ is frozen in with varying amounts of charges concentrated near the YSZ/Si interface.

Also at 80 K, the variation in accumulation capacitance with frequency is smaller, yielding a dielectric constant of 27. This result is consistent with bulk measurements of the dielectric constant of YSZ which converge over a wide frequency range to approximately the same value at low temperature.[11] The effect in the bulk is attributed to anion immobilization, and we suspect the same mechanism is influencing our devices.

Analysis of the *C-V* stretch-out at high frequency reveals a density of interface traps of about 3×10^{11} eV^{-1} cm^{-2} at midgap. This is about a factor of 3 lower than earlier measurements on ion beam sputtered YSZ/Si films.[13] We conjecture that our lower interface state density is caused by the 5 nm silicon oxide layer which forms at the YSZ/Si interface; the oxide layer may be absent in the prior work[13] because their oxygen growth pressure is ~600 times lower than that in our work.[2] Without an interfacial silicon oxide layer, the −6% lattice mismatch of the YSZ layer would presumably result in an increased number of interface traps.

Figure 4 also shows a comparison of low-temperature curves in the positive and negative voltage sweep directions. The positive sweep curve yields a lower capacitance due to insufficient generation of minority carriers, resulting in partial deep depletion. Variation of sweep rates leads to the conclusion that the inversion capacitance of the negative voltage sweep is overestimated due to the stagnant inversion layer.[15] The true inversion capacitance may be estimated from the positive sweep curves. The resulting value is less than that at room temperature. From computations based on the depletion approximation, and assuming complete dopant ionization at room temperature, we obtain a value of about 10^{16} cm^{-3} for the substrate doping and 70% dopant ionization at 80 K. This is within the range of the estimated doping concentrations in the boron-doped Si substrates.

In summary, a simple MIS structure has been successfully fabricated using a YBCO superconducting gate. The electrical measurements reveal that while the YSZ buffer layer is sufficiently insulating at superconducting temperatures, the effect of ions in this layer and at the insulator/semiconductor interface constitutes the key in understanding the device operation. Our findings do not seem to be dependent on the exact nature of the transition between the normal and superconducting states, nor are they directly influenced by the superconducting property of YBCO. Studies of this transition with capacitance measurements and comparisons between this structure and similar normal-metal gate structures are in progress.

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