Electrical Properties of Rapid Thermal Oxides on $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ Films

L. K. Bera
W. K. Choi
W. Feng
Cary Y. Yang
Santa Clara University, cyang@scu.edu
J. Mi

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Electrical properties of rapid thermal oxides on Si$_{1-x-y}$Ge$_x$C$_y$ films

L. K. Bera, W. K. Choi, and W. Feng

Microelectronics Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, 4 Engineering Drive 3, Singapore 117576

C. Y. Yang and J. Mi

Microelectronics Laboratory, Santa Clara University, 500 El Camino Real, Santa Clara, California 95053

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The electrical characteristics of rapid thermal oxides on Si$_{1-x-y}$Ge$_x$C$_y$ layers are reported. X-ray photoelectron spectroscopy results indicate segregation of Ge at the SiO$_2$/Si$_{1-x-y}$Ge$_x$C$_y$ interface, a thin GeO$_2$ layer at the oxide surface, and elemental Ge at the interface and in the oxide. The interface state density of the samples ranges from $3.0 \times 10^{11}$ to $3.6 \times 10^{12}$ eV$^{-1}$ cm$^{-2}$. All the samples show electron trapping behavior and the trap generation rate decreases with increasing C concentration. The charge-to-breakdown value and the oxide breakdown field are higher for Si$_{1.887}$Ge$_{0.113}$ than for Si$_{1-x-y}$Ge$_x$C$_y$ samples, and these values decrease with increasing C concentration. © 2000 American Institute of Physics. [S0003-6951(00)01928-8]

Heterojunction bipolar transistors, field effect transistors, and photodetectors based on Si$_{1-x-y}$Ge$_x$C$_y$ layers have been fabricated recently. In the realization of Si and Si-based heterojunction field effect transistors, oxidation is one of the most crucial process steps. Research in thermal processes has been suggested to be suitable for Si-based oxide charge ($Q_f$) and interface state density ($D_{it}$). Rapid thermal processing has been reported to be suitable for Si$_{1-x-y}$Ge$_x$ strained layer as it creates less misfit dislocations. In this letter, we examine the effects of Ge segregation and the role of C on the electrical properties of rapid thermal oxides (RTO) on Si$_{1-x-y}$Ge$_x$C$_y$ films.

The Si$_{1-x-y}$Ge$_x$C$_y$ samples were grown on n-type (100) Si substrates in a rapid thermal chemical vapor deposition (RTCVD) system. RTO was carried out at 1000°C in dry oxygen ambient for 270 s for all the samples. The oxide thickness was found to be between 10 and 16 nm. Details of the growth procedure and RTO process can be found in Refs. 7 and 8, respectively. The electrical properties of the oxides were obtained from the capacitance–voltage, conductance–voltage, current–voltage, and constant current stressing characteristics of an aluminum gate metal–oxide–semiconductor (MOS) capacitor structure.

Figure 1 shows an x-ray photoelectron spectroscopy (XPS) result of a RTO Si$_{0.8866}$Ge$_{0.113}$C$_{0.0184}$ sample. The peaks at the surface of the oxide correspond to the O 2s peak at 25.0 eV and the smaller and broader GeO$_2$ peak at 33.7 eV. The thin GeO$_2$ layer at the oxide surface has been identified previously at 1221.43 eV. By focusing on the Ge 3d peak (29.2 eV), one can see from Fig. 1 that elemental Ge is present throughout the oxide layer. This is not observable with the Ge 2p peak. The strong Ge 3d peak at the SiO$_2$/Si$_{1-x-y}$Ge$_x$C$_y$ interface (at profile time 1250–1500 s) confirmed the segregation of Ge at the interface. Riley and Hall reported a small amount of elemental Ge in anodized oxide on Si$_{0.84}$Ge$_{0.16}$ alloy film. In contrast, Fig. 1 shows a significantly higher elemental Ge concentration at the bulk and surface of SiO$_2$.

Figure 2 shows the high frequency (1 MHz) capacitance versus voltage characteristics of all the RTO samples. The inversion capacitance values ($C_i$) are higher for the Si$_{1-x-y}$Ge$_x$C$_y$ than Si$_{0.887}$Ge$_{0.113}$ samples. $C_i$ of the Si$_{1-x-y}$Ge$_x$C$_y$ samples increases with increasing C concentration. As $C_i$ can be increased with an increase in donor concentration in the semiconductor of a MOS capacitor, the increase in $C_i$ of the Si$_{1-x-y}$Ge$_x$C$_y$ samples may be due to an increase of donor-like centers in these films. This is possible as donor-like centers could be formed with the introduction of carbon into the SiGe network and the concentration of such centers increases with increasing C concentration.

$Q_f$ is calculated from the flatband voltage of Fig. 2 to be: $-9.53 \times 10^{10}$, $-1.4 \times 10^{12}$, $-2.2 \times 10^{12}$, and $-9.5 \times 10^{11}$ cm$^{-2}$ for samples Si$_{0.887}$Ge$_{0.113}$, Si$_{0.881}$Ge$_{0.113}$C$_{0.0059}$, Si$_{0.873}$Ge$_{0.113}$C$_{0.0132}$, and Si$_{0.8686}$Ge$_{0.113}$C$_{0.0184}$, respectively. $Q_f$ therefore increases with C in Si$_{1-x-y}$Ge$_x$C$_y$ films. Ahn et al. suggested that Si–O–Si and Si–O–Ge bonds can form during oxidation of the SiGe layer. The Ge–O bond is weaker and can be broken leaving a Si–O–dangling bond structure. If such dangling bond does not subsequently bond with another Si atom, it

*Electronic mail: elechoi@nus.edu.sg

FIG. 1. XPS spectra of the rapid thermal oxide grown on Si$_{0.8866}$Ge$_{0.113}$C$_{0.0184}$ film at 1000°C for 270 s. Note that the SiO$_2$ region covers from profile time 0 to 1250 s.
can trap an electron and becomes negatively charged. Our XPS results show that the Ge 3d peak intensity is lower for RTO $Si_{0.887}Ge_{0.113}$ than for $Si_{1-x-y}Ge_{x}C_{y}$ samples. This means that the elemental Ge content in the oxide and in the SiO$_2$/substrate interface is lower in $Si_{0.887}Ge_{0.113}$ than the $Si_{1-x-y}Ge_{x}C_{y}$ samples. If the elemental Ge originates from Ge atom detached from the Si–O–Ge bond, then the elemental Ge concentration should be related to $Q_f$. This agrees with our $Q_f$ results presented in Fig. 2.

The $D_{it}$ values of samples $Si_{0.887}Ge_{0.113}$, $Si_{0.8811}Ge_{0.113}C_{0.0059}$, $Si_{0.8738}Ge_{0.113}C_{0.0132}$, and $Si_{0.8686}Ge_{0.113}C_{0.0184}$ are calculated to be: 3.0 $\times$ 10$^{-11}$, 1.1 $\times$ 10$^{-12}$, 1.6 $\times$ 10$^{-12}$, and 3.6 $\times$ 10$^{-12}$ eV$^{-1}$ cm$^{-2}$, respectively. $D_{it}$ is higher for $Si_{1-x-y}Ge_{x}C_{y}$ samples compared to $Si_{0.887}Ge_{0.113}$ and increases with an increase in C concentration in the films. As the increase in the Ge pileup at the SiO$_2$/Si$_{1-x-y}Ge_{x}C_{y}$ interface will increase the misfit dislocation, $D_{it}$ is therefore directly related to the peak Ge concentration at the SiO$_2$/Si$_{1-x-y}Ge_{x}C_{y}$ interface.

Figure 3 shows the current versus field characteristics of the MOS capacitors measured under a positive gate bias condition. The breakdown field strength of oxide grown on Si$_{1-x-y}Ge_{x}C_{y}$ films was found to be in the range of 10–14 MV/cm. The oxide breakdown field reduces as the C concentration in the Si$_{1-x-y}Ge_{x}C_{y}$ substrate increases. The SiO$_2$/Si$_{1-x-y}Ge_{x}C_{y}$ barrier heights extracted from Fig. 3 were found to be 3.48, 3.07, 2.72, and 2.82 eV for samples $Si_{0.887}Ge_{0.113}$, $Si_{0.8811}Ge_{0.113}C_{0.0059}$, $Si_{0.8738}Ge_{0.113}C_{0.0132}$, and $Si_{0.8686}Ge_{0.113}C_{0.0184}$, respectively. Cross-sectional transmission electron microscopy results showed that the rough SiO$_2$/Si$_{1-x-y}Ge_{x}C_{y}$ interface for higher C content samples. We believe this rough interface results in higher electric field and thus a lower effective barrier height.

We monitored the change of gate voltage ($\Delta V_G$) of the MOS capacitors for a constant current 30 nA/cm$^2$ with positive bias to the Al gate. The positive $\Delta V_G$ shift for all the samples in Fig. 4(a) shows electron trapping characteristics. The electron trap generation is higher for $Si_{0.887}Ge_{0.113}$ than the $Si_{1-x-y}Ge_{x}C_{y}$ samples, and the trap generation rate decreases with increasing C concentration in the films. Our secondary ion mass spectroscopy results showed that during RTO of Si$_{1-x-y}Ge_{x}C_{y}$ samples, some of the C is consumed via formation of CO$_2$ or CO and the rest remains in the oxide. Carbon atoms in the oxide have been reported to act as positive charges. All these nonsubstitutional C contributes to hole traps, and hence, decreases electron trap generation. Figure 4(b) shows that the charge to breakdown value of $Si_{0.887}Ge_{0.113}$ sample is higher compared to $Si_{1-x-y}Ge_{x}C_{y}$ samples. For the Si$_{1-x-y}Ge_{x}C_{y}$ samples, the charge to breakdown value decreases with an increase in the C concentration. During oxidation the outdiffusion of C atoms may cause conducting path between the interfaces to be formed via randomly generated traps in the oxide. Such conducting path will reduce the charge to breakdown value of the film.

**FIG. 2.** High frequency (1 MHz) capacitance–voltage characteristics of Al–SiO$_2$–Si$_{1-x-y}Ge_{x}C_{y}$ and Al–SiO$_2$–Si$_{1-x}Ge_{x}$ capacitors.

**FIG. 3.** Current vs electric field characteristics of Al–SiO$_2$–Si$_{1-x-y}Ge_{x}C_{y}$ and Al–SiO$_2$–Si$_{1-x}Ge_{x}$ capacitors. Note that the Al contact area is 3.14 $\times$ 10$^{-4}$ cm$^2$.

**FIG. 4.** (a) Gate voltage shift vs stress time characteristics of RTO on Si$_{1-x-y}Ge_{x}C_{y}$ and Si$_{1-x}Ge_{x}$ films. The samples were under a constant current stress of 30 nA/cm$^2$. (b) Charge-to-breakdown characteristics of RTO on Si$_{1-x-y}Ge_{x}C_{y}$ and Si$_{1-x}Ge_{x}$ films. Note that the initial voltage value (at time zero) is set by the oxide thickness.
Also the probability of forming conducting path increases with increase in the C concentration in the film.

In conclusion, our XPS results revealed that elemental Ge exist in the oxide and oxide/alloy interface. $Q_f$ and $D_{it}$ increase, but the breakdown field, effective barrier height, and charge-to-breakdown values decrease, with increasing C concentration in the $Si_{1-x-y}Ge_xC_y$ films. The oxides exhibit electron trapping behavior and the trap generation rate decreases with an increase in C concentration in the film.

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