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Wireless Multi-User Communication System

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ABSTRACT

The project's ultimate goal is to send and receive information wirelessly from multiple unique users at once. Our design includes an antenna with beam-switching capabilities to serve multiple users at once. The project also focused on providing a more compact solution along with additional uplink capability and power indication. This has the potential to be used in the upcoming 5G machine to machine communication. The antenna and feed network were made smaller by making use of less conventional structures. The power indicator was made by using a digital logic circuit. These components form a proof-of-concept communication system.

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- Jonathan Lee, Master's in Electrical Engineering at Santa Clara University, for allowing us to continue the project
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1 Introduction

1.1 Background

60% of the world still lacks access to the internet which means that the majority of people are put at a disadvantage in terms of educational, social and economic opportunity. Most of these people live in extremely rural and poor areas. A specific solution that focuses on low cost internet access and usability in this environment is needed in order to tackle the problem. The environment often has poor existing infrastructure, limited electricity/power and is generally inconvenient. To address this, we created an implementation that is wireless, mobile in size and low-power.

With the appearance of cheap sensors and wireless components, IoT (internet of things) devices are becoming more prevalent in everyday life. However, there is not enough bandwidth to accommodate all devices at once. The upcoming 5G network will implement machine to machine communication in many devices which will significantly increase data use. It becomes necessary to prioritize certain devices over others in order to complete urgent tasks faster. The project aims to create a device that can transmit a narrow beam of signal to different directions in order to meet this need. A beamforming network was created that consists of the hub and the user which can support 2-way communication. The hub is able to be automatically controlled in order to pick which user it wants to serve.

Extensive knowledge in radio frequency (RF) courses as well as in preliminary courses was necessary for this project. Graduate level RF courses helped a lot in understanding the different parameters, interpreting measurements, and designing RF structures. Such classes that helped us in our project were ELEN 21 (Introduction to Logic Design), ELEN 115 (Electronic Circuits I), ELEN 105 (Electromagnetics II), ELEN 706 (Microwave Circuit Analysis and Design), ELEN 624 (Signal Integrity), and ELEN 715 (Antennas I). A broad electrical engineering knowledge overall was necessary to work with digital circuits and pre-bought components. New skills were also needed to ensure a successful project. New CAD tools had to be learned and familiarity with old CAD tools also had to be polished. We used 5 different CAD tools in this project: ANSYS HFSS, ADS, Eagle, LTSpice and Diptrace. A lot of research was also spent looking into RF structure in order to make the size smaller.

1.2 Project Objectives and Requirements

Being able to switch the main lobe is important to prioritize the needs of different users. Some users may need more data than others. The beamforming network can switch the beam to direct it at different users for different lengths of time. This feature was already implemented by the previous project. Our project is a continuation of a previous project.

It continued where they left off and added more features as well as improved existing features. We added on a communication link between the transmitter and receiver which means that there will be downlink as well as uplink in order to exchange information. The antenna system on the user end will also be improved/replaced to be smaller while still having acceptable performance. We also need a logic network in order to light an LED at the receiver end. The reason we need a logic network is so that the lights can turn on without the use of a microcontroller. Theres no need for something as fancy as a microcontroller to light a few LEDs. If it was mass produced then using a simple logic network would be much cheaper and power efficient than using a microcontroller.

The power indicator needs to have at least 4 LEDs to indicate signal reception to imitate how a phone is able to. It also should not use a microcontroller for reasons mentioned previously. The downlink and uplink must work between 5.725 GHz and 5.875 GHz because it is part of the 5.8 GHz ISM band. The new components must still keep the capabilities of the old component such as being able to switch between 4 different directions at around the same gain. The components must be small enough to be handheld. The antenna needs to have a reflection coefficient of less than -10 dB and a gain of higher than 3 dB.

1.3 Design Alternatives Considered

Originally, we had two possible implementations for the power indicator: one is implementing a graphical user interface (GUI), and another is a circuit consisting of comparators and diodes. A GUI would be pretty convenient to use since no extra hardware is required, and that the microcontroller can be used, but the problem to that was the lack of experience in making GUIs, and the time to make one given our experience. Another option as we have mentioned is to use the logic gate LED network (which we selected). Fortunately, for this system, we can improve it once we have the baseline down, but as we design and improve it, we have to take the design complexity and the defective parts into account when designing the printed circuit board (PCB).

For the patch antenna, we can use a half-wave patch but the alternative is to use a quarter-wave patch which offers area reduction needed. For the transmission line, we have considered two implementations: the artificial transmission line (ATL), and a regular wave transmission line. If we use the artificial transmission line, we can make our system smaller, but its harder to make, and doesnt behave as nice since it is just a model. The second implementation that we have considered is just a regular quarter wave transmission line, which is easier to make and that its behavior is well-known and simple. Unfortunately, we have to design it at a specific length and it will take up more space.

Besides the transmission line, we plan to implement a phase shifter, which can be either variable or fixed. A variable phase shifter can sweep the main lobes direction between angles, and can be purchased. However, they are quite expensive and we still need to figure out how to integrate them onto the board design. On the other hand, a fixed phase shifter is smaller and cheaper, but can only be set at certain directions, and that we have to make it ourselves.

Finally, we have considered using an RF filter in our design to differentiate the uplink signal from that of the downlink more easily. However, it is very difficult to find narrow band-pass filter at such a high frequency, so we may have to design it in case. In fact, we may not need the RF filter, which makes our system simpler.

1.4 Final Design Selection

We have decided to stick with the logic network design for the power indicator, as we have more experience in logic design and electronics. In order to make other parts of the board smaller, we have decided to delve into metamaterials. Instead of a conventional transmission line, we will use periodic loaded transmission lines to shorten the length. An ATL is a kind of periodic loaded transmission line. We did not use a variable IC phase shifter because it cannot be used for both downlink and uplink.

When designing the logic-based power indicator, one of the risks is that we may not necessarily find the components that may comply to our design criteria. Fortunately, the risk is pretty low, as the software used to model the logic network has a huge library of components. More importantly, the biggest risk in the physical design is the defectiveness of the components. To reduce the impact, we plan to start on it over the break, and finalize it by the end of week 3 of winter quarter.

Perhaps the riskiest part of this project is using metamaterials to reduce the size of the beamforming network. Initial design of the ATL has failed because it turned out that the design didn't make the transmission lines smaller when implemented at high frequencies.

2 System Overview

2.1 Overall System Overview

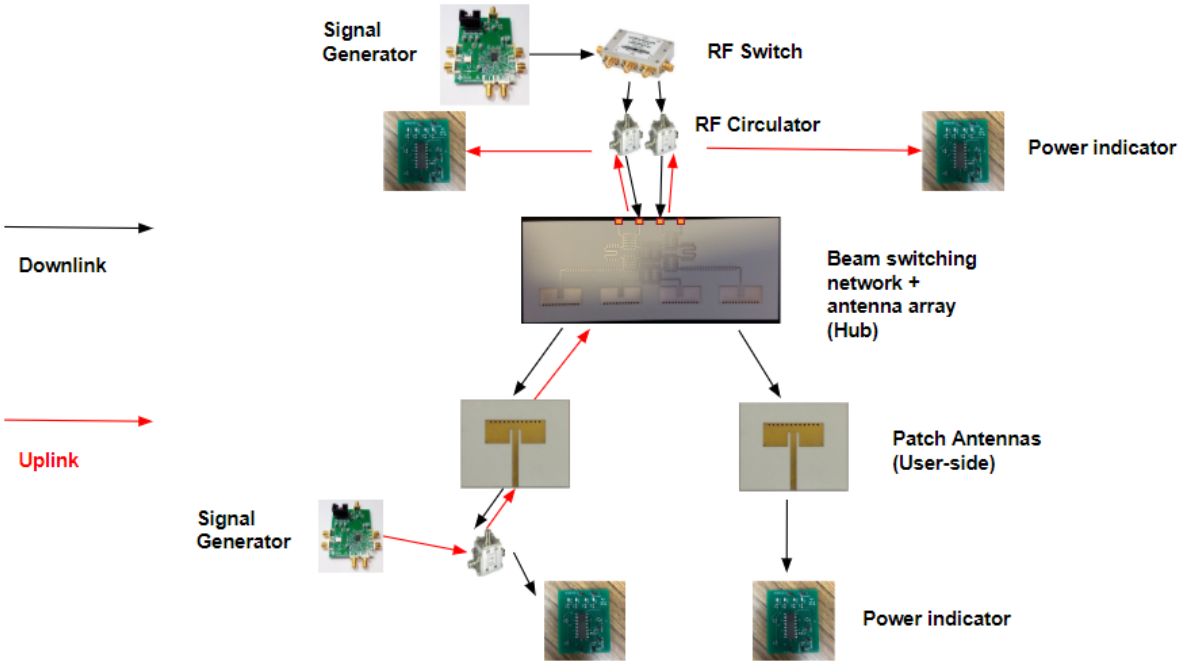


Figure 2.1: Overall Diagram of the Communication System

The communication system consists of the hub and the user side. The hub is the upper half of the diagram while the user side is the lower half. Both the hub and user side are capable of transmitting and receiving thanks to the RF circulator. However, the difference is that the hub is capable of being controlled. There is a laptop that connects to the RF switch in order to excite different ports of our choosing. That will enable the hub to direct the main lobe in different directions to different users. The power indicator will visually indicate signal reception.

2.2 Component Overview

2.2.1 RF Switch

The RF switch is the Mini Circuits USB-SP4T-63. It receives an input signal and sends it to one of its 4 output ports depending on the selection made in the software. The software is installed on a laptop and can be interacted with a GUI. The RF switch is also programmable using C but that feature was not used in this project.

2.2.2 RF Circulator

The RF circulator is the main component responsible for enabling both uplink and downlink in the system. The RF circulator is a ferromagnetic 3-port device. Usually, it does not matter which way a signal goes through a wire. The characteristic impedance of the transmission line for the forward waves in both directions will be the same. With an RF circulator, a signal will be able to travel in one direction but will have almost all the signal going in the opposite

direction attenuated. When the RF circulator is connected to an antenna, it allows the system to both send and receive signals using the same antenna and make sure that the sent and received signals do not interfere with each other. The isolation between the circulator ports we had and tested in the lab were better than 17dB at our design frequency. The measurement plot of the circulators are shown in appendix and are not presented here for brevity. The actual measurement results from lab agrees with the data sheet and confirms that it is working properly.

2.2.3 RF to DC Converter

This component is not shown on the diagram but could be considered as part of the power indicator. The RF to DC converter takes in an RF input and outputs a corresponding DC voltage. The DC voltage is then used as the input for the power indicators.

The other components such as the hub, patch antennas and power indicator will be discussed in depth in their own chapters.

3 Design Solution: Patch Antenna

3.1 Background

The patch antenna is the component that enables EM waves to propagate into free space. The typical patch antenna is called the half-wave patch antenna. The patch antenna is made of copper traces on top of a dielectric substrate with a GND plane at the bottom of the substrate (See Fig. 3.1). The starting equations for the length and width of the patch antenna is shown [1].

$$W = \frac{\lambda}{2}\left[\frac{\varepsilon_r + 1}{2}\right]^{-1/2} \tag{3.1}$$

$$L \approx 0.49\lambda_d = 0.49\frac{\lambda}{\sqrt{\varepsilon_r}} \tag{3.2}$$

Here, λ_d is the wavelength in the dielectric substrate which is different from the free space wavelength because of the dielectric constant of the substrate (dielectric constant is close to 1 in air).

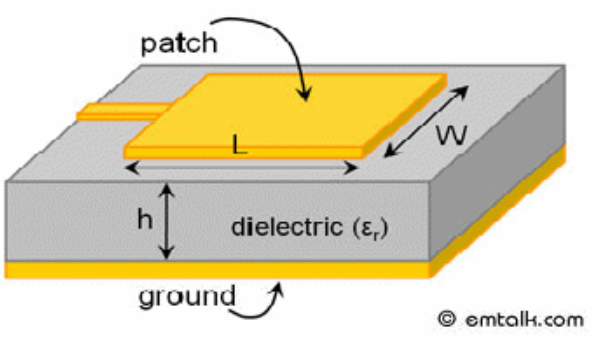


Figure 3.1: Here's how the patch antenna looks like [2].

3.2 Implementation Detail

This project makes use of a particular type of patch antenna called the quarter-wave patch antenna in order to reduce the size. As the name implies, the length of the antenna is reduced by roughly half its size while the width stays roughly the same. This is done by physically shorting the half wave patch in the middle and then removing the other half of the antenna. There is a virtual GND at the midpoint of the half wave patch antenna. The quarter wave patch antenna essentially forces that location to be a GND by physically shorting it and so the upper edge of the quarter wave patch antenna is shorted to GND. If there is no physical GND and the patch antenna length is varied then the virtual GND will move around as well which is not what we want. Since the upper edge of the quarter wave patch is grounded, there is only 1 radiating edge which is the bottom edge of the quarter wave patch. A regular half wave patch has 2 radiating edges; one at the bottom edge and one at the top edge.

There are 2 ways to implement the physical shorting to GND. The simplest way is to have a wall of copper metal going straight to GND. While this is easy to model and simulate on a CAD software, most PCB fab house will have difficulty making this structure. Another way is to use plated through-hole vias going straight to GND. This is very easy to make for the PCB fab house but the downside is that this will make the antenna slightly longer based on the diameter of the vias. The vias also have inductance and will introduce a positive input impedance to the antenna. This will make matching the antenna to the port more difficult. A gap which acts as a microstrip capacitor was used right before the input to the antenna in order to counteract the inductive effect.

Another problem with the antenna is the high input impedance at the edge of the antenna. A quarter wave transformer can be used to match the edge of the antenna to the 50 Ω port with the following equation [3]:

$$Z_{in} = \frac{Z_0^2}{Z_L} \tag{3.3}$$

where Z_{in} is the impedance of the port, Z_L the edge impedance of the antenna, and Z_0 the impedance of the transmission line which makes up the quarter wave transformer itself. A high antenna impedance (Z_L) means that the quarter wave transformer impedance (Z_0) also needs to be high. It turns out that the Z_0 ended up becoming too high which requires the transmission line to be very thin. It was too thin for the PCB fab house to make so a different type of feed was needed.

An inset feed was used to connect to the antenna instead. The impedance of the antenna will drop as you look further into the antenna from the edge. The distance of this inset was determined using optimization until the antenna input impedance is 50 ohms. A 50 ohm transmission line is then connected to the input of the antenna. A transmission line of this impedance is wide enough to be comfortably fabricated by the PCB fab house.

3.3 Simulation Results

The layout of the quarter wave patch antenna is shown in Fig. 3.2 using ANSYS HFSS. The simulation result of the S_{11} parameter plot is also shown The S_{11} is around −9.2 dB at 5.8 GHz and is resonant at around 5.83 GHz.At first the simulation results were much better but it was found that there was a mistake with the antenna model. In order to model the plated through-hole vias, a copper cylinder with the center removed was used which leaves only a thin wall of copper plating. The center of the vias was supposed to be filled with air. However, we only put holes in the copper cylinder in ANSYS HFSS and not the other layers such as substrate, GND plane and signal plane. This meant that the initial simulation results using HFSS had the vias filled with Rogers RO4350B substrate and no holes in the signal and GND plane which is not what was expected. The initial simulation results after the layout was corrected are shown in Figures 3.3 and 3.4. Fig. 3.3 shows S_{11} parameter which is basically reflection coefficient at the input port of the feed line. Fig. 3.4 shows the 2D cut planes of the antenna radiation pattern in $\phi = 0$ and $\phi = 90$ degrees. The radiation pattern plots are polar plots that show how the radiated power (represented with antenna gain in Fig. 3.4) is distributed in space.

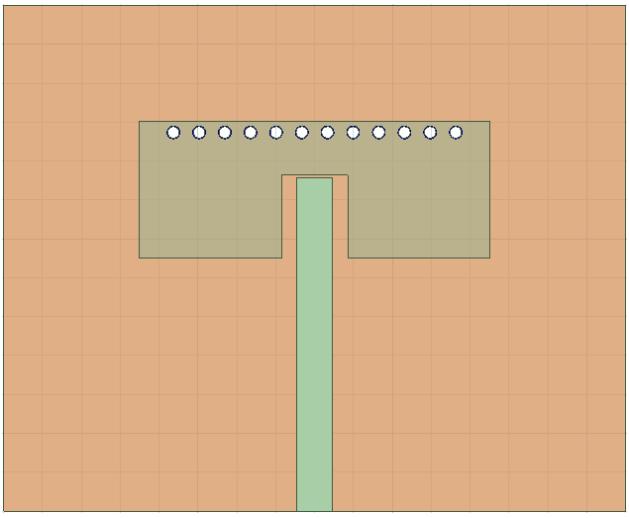


Figure 3.2: User-side quarter wave patch antenna made on ANSYS HFSS.

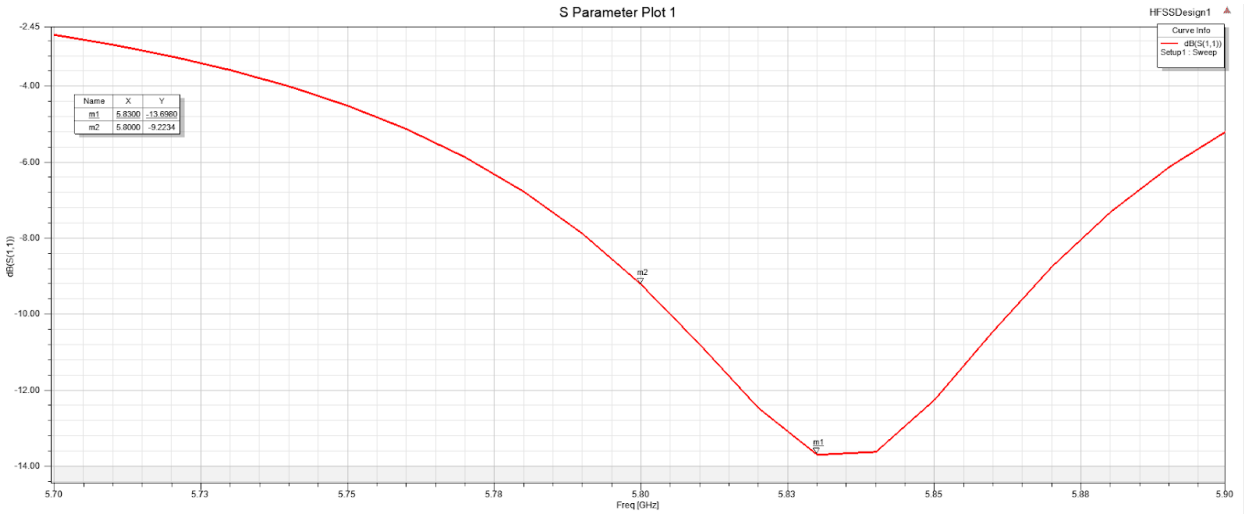


Figure 3.3: S_{11} Parameter Plot from simulation on HFSS.

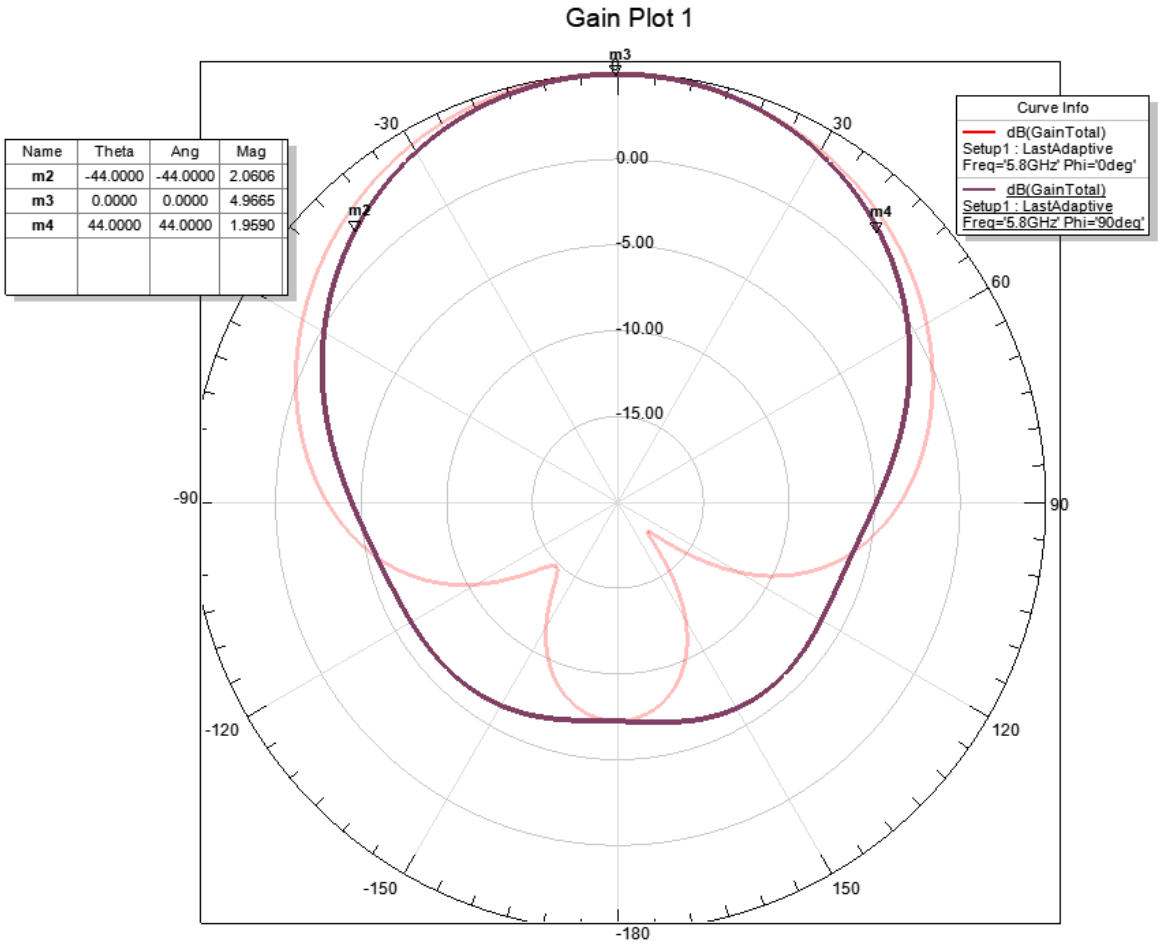


Figure 3.4: Radiation Plot from simulation on HFSS.

3.4 Fabrication Results

Actual fabrication and its results are shown below. The substrate material chosen is Rogers RO4350B. This was chosen because it can be used in the same fabrication process as the common FR4. It also has superior performance because of lower losses, more consistent dielectric constant across different frequencies and more consistent dielectric throughout the board area. The final width and length of the patch antenna (Figure 3.5) is 18 mm and 7.06 mm, respectively. The small gap which acts like a microstrip capacitor is 0.12 mm. This reduces the antenna area by about 30% relative to that of the old antenna, as shown in Figure 3.6. Ideally the area would be halved but Rogers RO4350B has a smaller dielectric than FR4 so the length has to be slightly larger. There is also an extra length introduced because of the diameter of the vias.

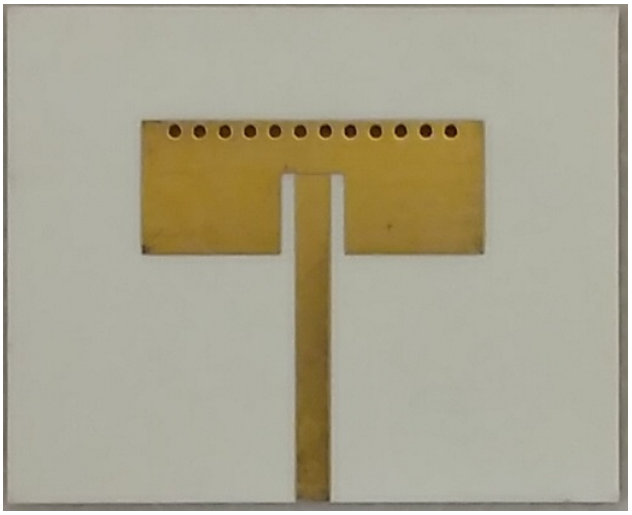


Figure 3.5: Actual user-side antenna from fabrication.

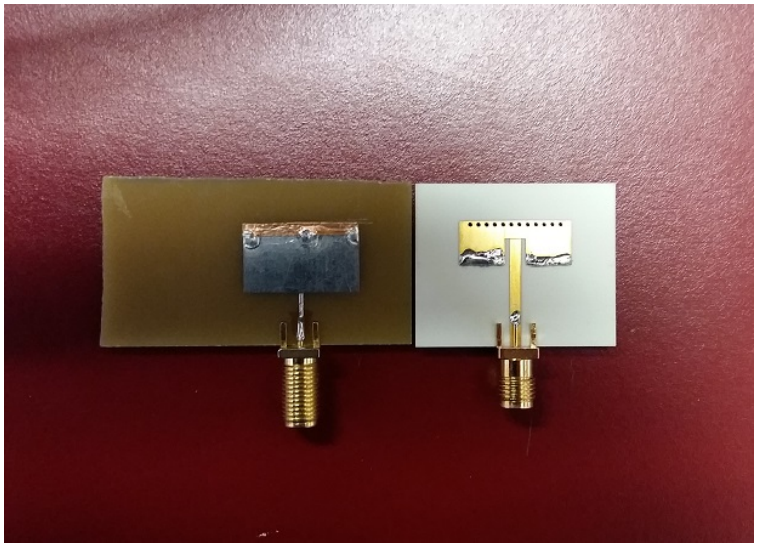


Figure 3.6: Size comparison between old (left) and new patch antenna (right)

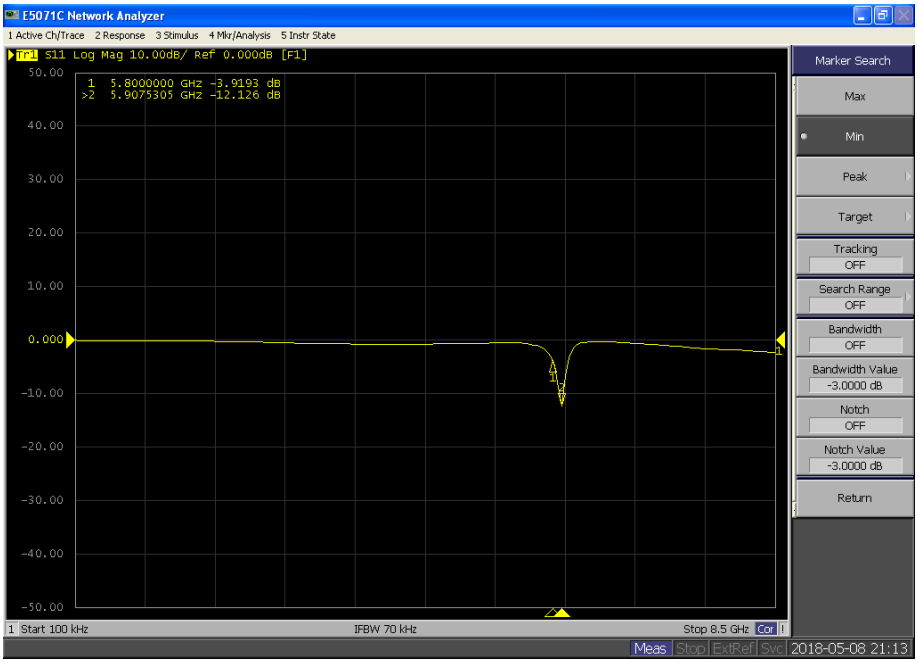


Figure 3.7: S_{11} parameter plot from VNA measurement before copper tape fixing.

Fig. 3.7 shows the measured S_{11} of the fabricated prototype using a vector network analyzer (VNA). It can be seen that even after fixing the problems in the simulation that the actual S_{11} parameter results are somewhat different from the simulation results. It is resonant at 5.907 GHz instead of 5.83 GHz in the simulation and even further than the 5.8 GHz that we want. The patch antenna was made slightly longer using copper tape fixing in order to move the center frequency to 5.8 GHz. The result of the copper tape fixing is shown below.

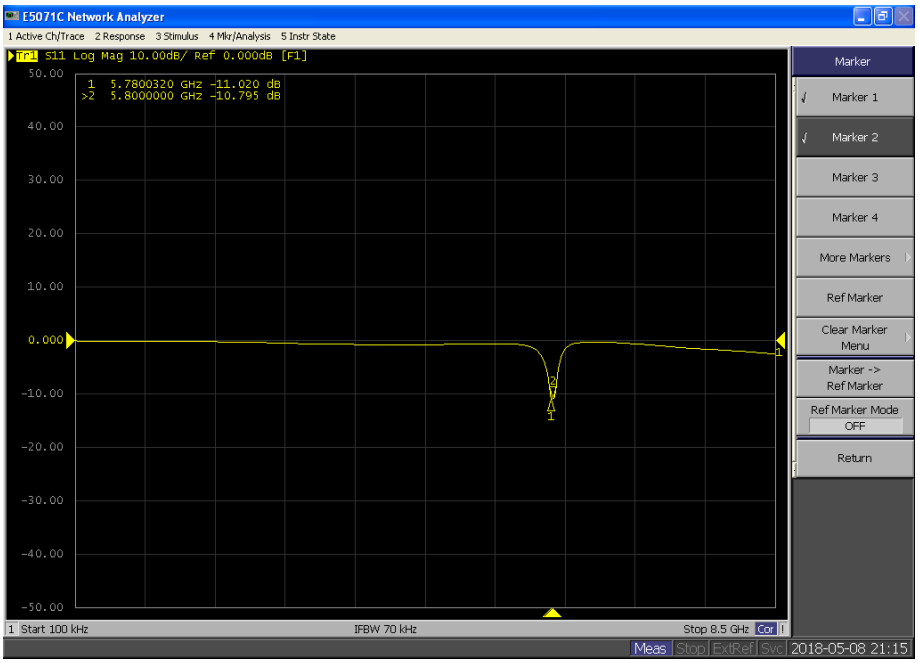


Figure 3.8: S_{11} parameter plot from VNA measurement after copper tape fixing.

The S_{11} parameter is below -10 dB at 5.8 GHz which meets our requirement.

4 Design Solution: Power Indicator

4.1 Phase 1: Design and Simulation

The power indicator consists of a set of comparators such that their negative inputs are voltages determined by a resistive voltage divider network. The positive inputs are a DC voltage from the RF to DC converter. Moreover, their outputs are connected to a diode in series with a current limiting resistor. The power indicator is designed such that when the positive input increases, the diodes would turn off. This is due to the fact that the RF to DC converter outputs a smaller DC voltage for a higher RF power.

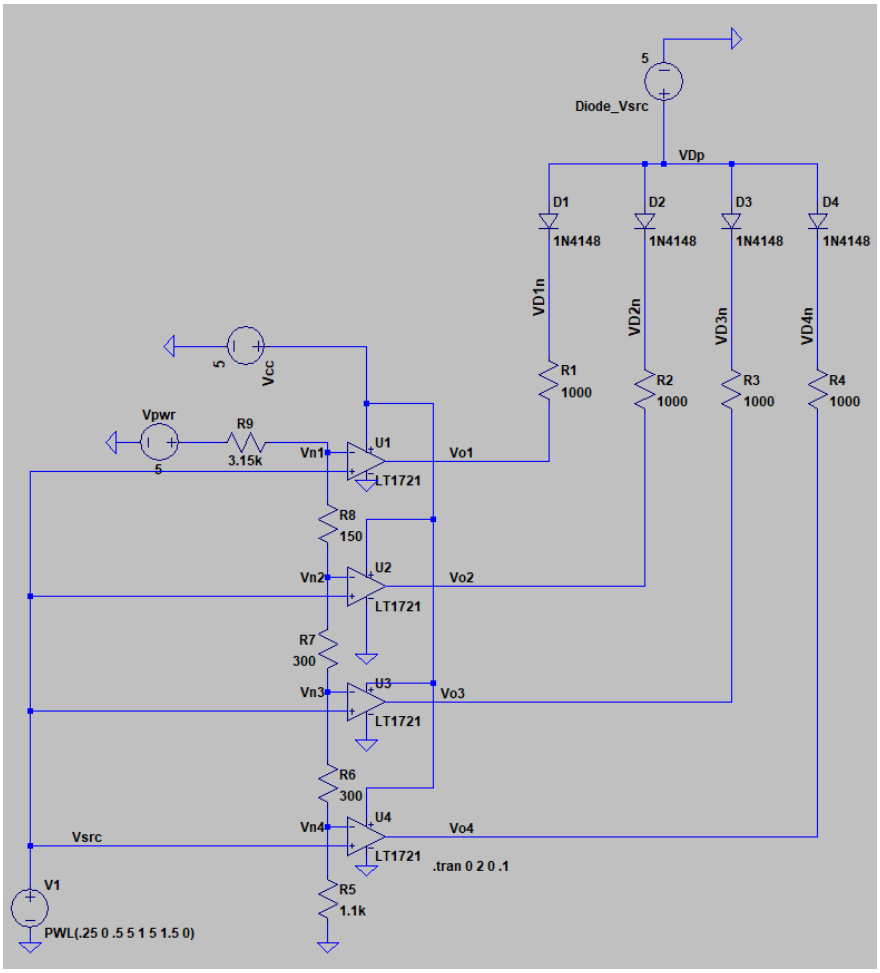


Figure 4.1: Schematic of the power indicator on LTSpice.

Note that the threshold voltages can be adjusted by the voltage supply connected to the resistor network.

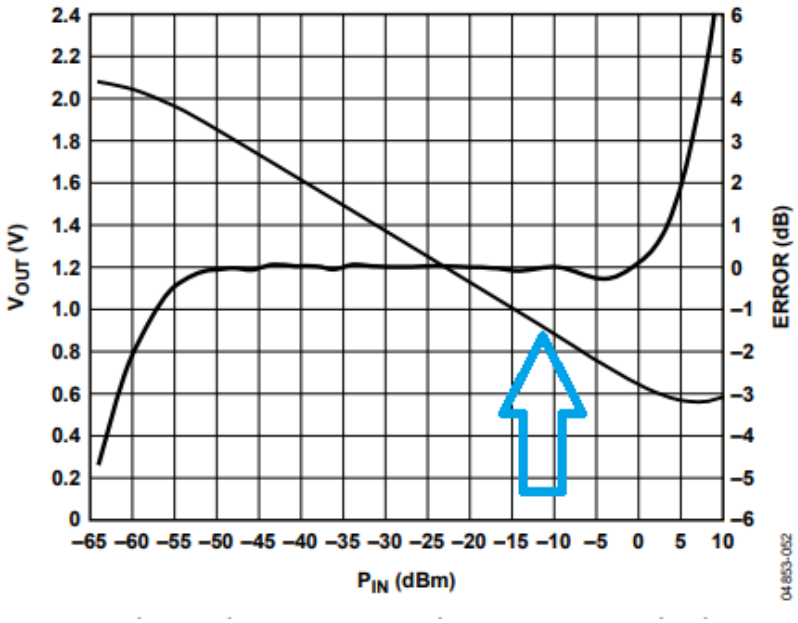


Figure 4.2: Relationship between RF power and DC voltage on the RF to DC converter, as indicated by the blue arrow [4].

We then applied a test pulse voltage to the positive output to verify the schematic's functionality.

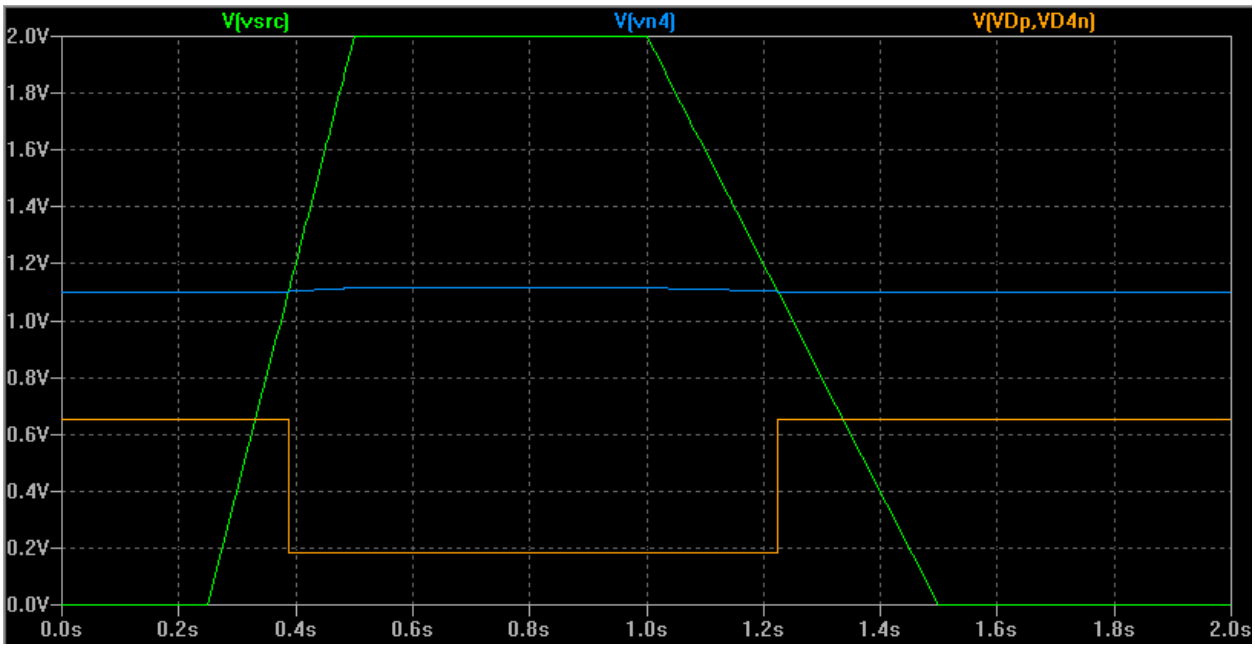


Figure 4.3: Plots of the test voltage (green), negative input on U4 from figure 4.1 (blue), and voltage across diode connected to U4 (orange).

As one can see from the plot, the diode is off when the test input is greater than the negative input, and on when it's the other way around. The functionality is therefore correct, according the plot.

4.2 Phase 2: Breadboard

The next step was to come up with a prototype of our power indicator. We did this by implementing the circuit on the breadboard. We then set the voltage supply for the resistor network to 5 volts as it was done in LTSpice. Next, we applied a test voltage and measured each threshold voltage three times, then averaged them.

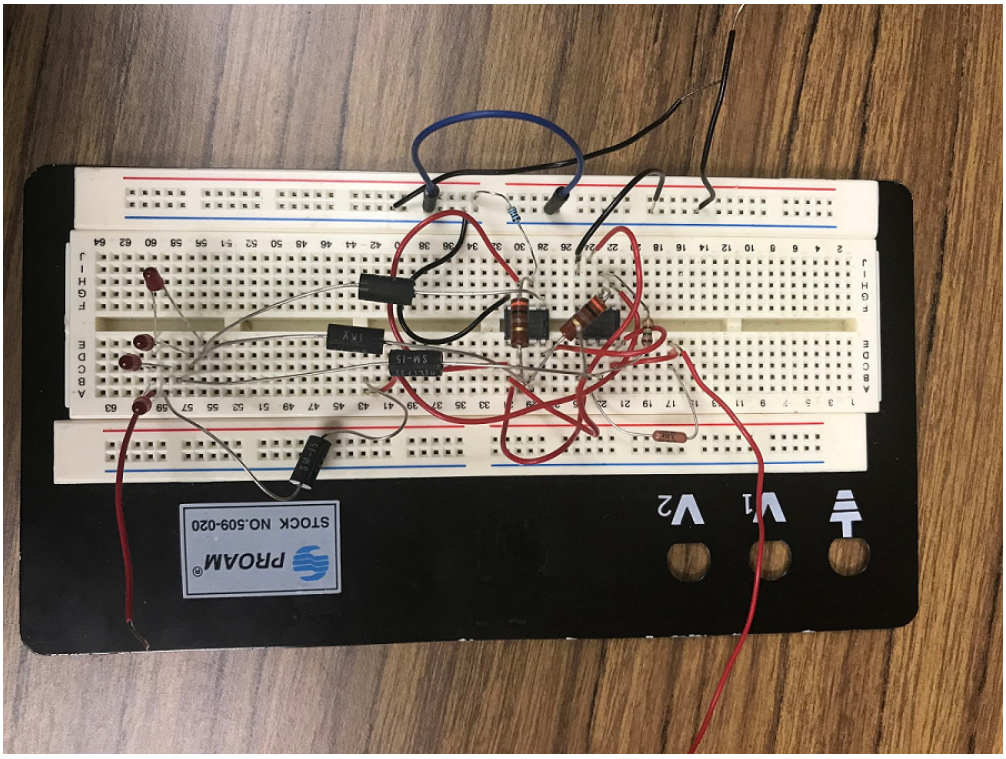


Figure 4.4: Implementation of the power indicator on the breadboard.

	Theoretical Values (volts)	*Actual Values (volts)*
4 to 3 LEDs	1.10	1.10
3 to 2 LEDs	1.40	1.41
2 to 1 LED	1.70	1.683
1 to 0 LEDs	1.85	1.856

Table 4.1: Table of theoretical and measured threshold values for power indicator on the breadboard.

The actual results in table 4.1 are consistent with the theoretical values, which means that the functionality of the breadboard implementation of the power indicator is correct. However, the breadboard implementation is not robust as a slight movement of any component can make a huge change in the circuitry. Therefore, we went on to implement the power indicator on the printed circuit board (PCB).

4.3 Phase 3: Printed Circuit Board (PCB)

We used Eagle for PCB design, then sent the gerber files to Royal Circuits for fabrication. We then bought the components necessary for the PCB and soldered them. However, we had to buy a 3.3 kΩ resistor instead of a 3.15 kΩ one because the latter did not have a package size appropriate to its designated footprint, while the former did.

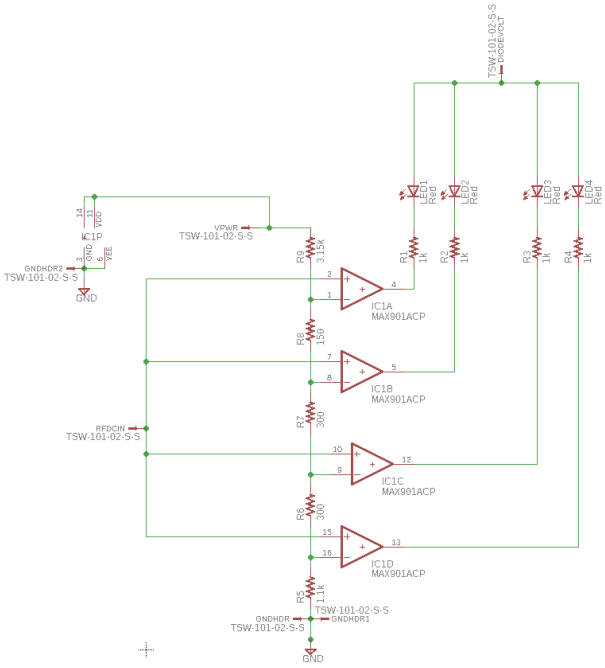


Figure 4.5: Schematic of the power indicator on Eagle.

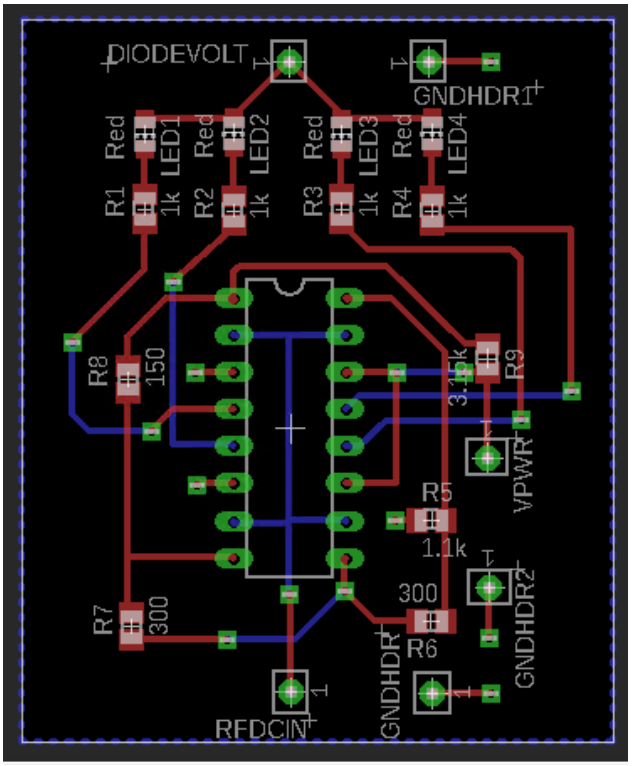


Figure 4.6: Layout of the power indicator on Eagle.

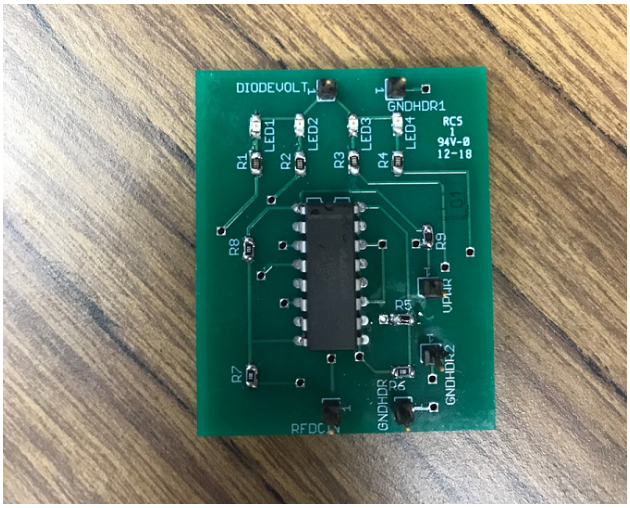


Figure 4.7: Power indicator fabricated on the PCB.

We then did the verification for the PCB like what we did for the breadboard.

	Theoretical Values (volts)	***Actual Values (volts)***
4 to 3 LEDs	1.07	1.073
3 to 2 LEDs	1.36	1.376
2 to 1 LED	1.65	1.65
1 to 0 LEDs	1.80	1.807

Table 4.2: Table of theoretical and measured threshold values for power indicator on the breadboard.

The actual results in table 4.2 are consistent with the theoretical values, which means that the functionality of the PCB implementation of the power indicator is correct. Given that the PCB is robust, this satisfies the objective of having power indication in our system.

5 Design Solution: Butler Matrix

5.1 Background

We have already met the original objectives of the project by having the uplink and downlink capability, a smaller patch antenna and the power indicator working. However, there was still some time remaining so we decided to push ourselves to reduce the size of the Butler matrix as well.

A 4×4 Butler matrix was made which acts as a feed to an array of 4 patch antennas. The Butler matrix which is passive routing network is shown in Fig. 5.1. It consists of 4 input ports and 4 output ports which is connected to the patch antennas. The function of the butler matrix is to provide the necessary phase shifts when the signal reaches the output ports from the input ports. What matters is not the final phase shift of the signal at one of the outputs but rather the phase difference between adjacent output ports. When the signals get launched into the air, the phase difference between the output ports will cause the signal to constructively and destructively interfere at certain angles in the far field. The resulting pattern will have a strong narrow beam at certain directions and almost no beam at the other directions in the ideal case. Changing the phase difference between the output ports will then allow you to have a narrow beam at different select angles. This concept is called beamforming.

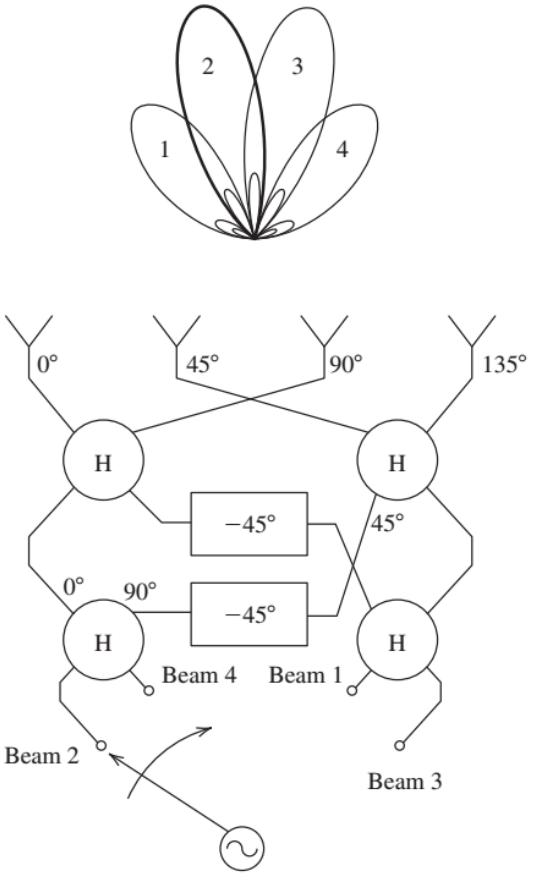


Figure 5.1: Functional Diagram of Butler Matrix [1].

Figure 5.1 shows that switching which input port to excite will change the phase difference between the output ports. This will result in changing the main beam direction as explained earlier. Switching which input ports to excite is done using an RF switch in our system and the RF switch is controlled using a laptop. The component labeled “H” in the figure is the quadrature hybrid. The quadrature hybrid splits power equally between its 2 output ports with a

phase difference of 90 degrees. The component labeled "−45°" cannot be implemented directly in real life because there cannot be a negative phase lag with passive components. To create the same effect using passive components, a 90 degree phase shifter, 45 degree phase shifter and a crossover is needed. Another name for the crossover is the 0 dB coupler shown in Figure 5.2 [5].

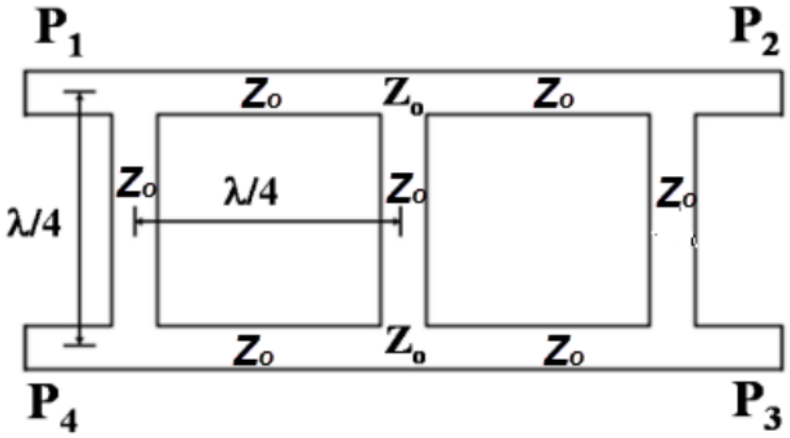


Figure 5.2: Layout of crossover.

The crossover works by receiving a signal at one of its ports and then sending it to a diagonal port. Ideally, there would be no signal going to the other 2 ports. For example, if signal is being sent to port 1 then almost all the signal should arrive at port 3 while almost none should be going to port 2 or port 4.

The butler matrix is then made up of a combination of 4 components; the quadrature hybrid, 45 and 90 degree phase shifters, and the crossover (0 dB coupler). Each of these components are made using transmission lines of a particular impedance and electrical length that are arranged in different manners. If the individual transmission lines can be made smaller then that would decrease the size of each of the 4 components which will then decrease the size of the entire butler matrix. A smarter placement of these transmission lines would also help in minimizing board size which is not always possible with regular transmission lines because they have to be of a certain width and length. The solution to these problems is to use a slow-wave structure called Artificial Transmission Line (ATL).

5.2 Artificial Transmission Line

An ATL is a type of slow wave structure. As the name implies, it is able to slow down the speed at which waves travel. This means you can have a physically shorter structure compared to a regular transmission line and still have the same electrical length. There are many types of ATLs. Two different structures were considered in this project but only one ended up working.

5.2.1 First Design

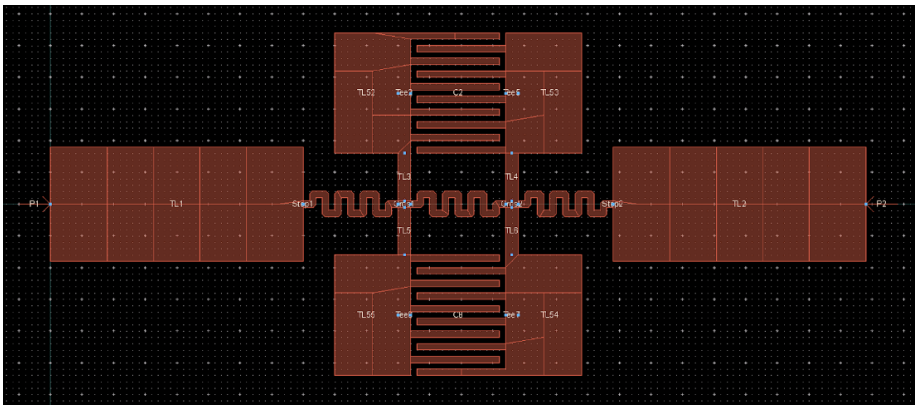


Figure 5.3: Layout of the first ATL design on ADS.

The initial design of the ATL as shown in Figure 5.3 did not work out as expected. Halfway between making the ATL, it was found that this design of ATL will grow too large for higher frequencies. This was probably why we could not find any papers that had parameters for higher frequency ATL of this type. This one was only at 1 GHz while we need it to work at 5.8 GHz. The parallel plate capacitors (the plates next to the inter-digital capacitors with finger-like structures) will grow too large at higher frequencies negating the reason we used it in the first place, to make the beamforming network smaller. This is because the capacitance has to increase in order to match the increase in inductance from the meandered line inductors (thin zig-zag lines). At higher frequencies, the meandered line inductors will become thinner and have higher inductance as an unwanted consequence. In contrary, a regular transmission line will become smaller as the frequency goes up because the wavelength becomes shorter. Even then, the simulation results were not very good at 1 GHz though this could be caused by the low mesh density.

5.2.2 Second Design

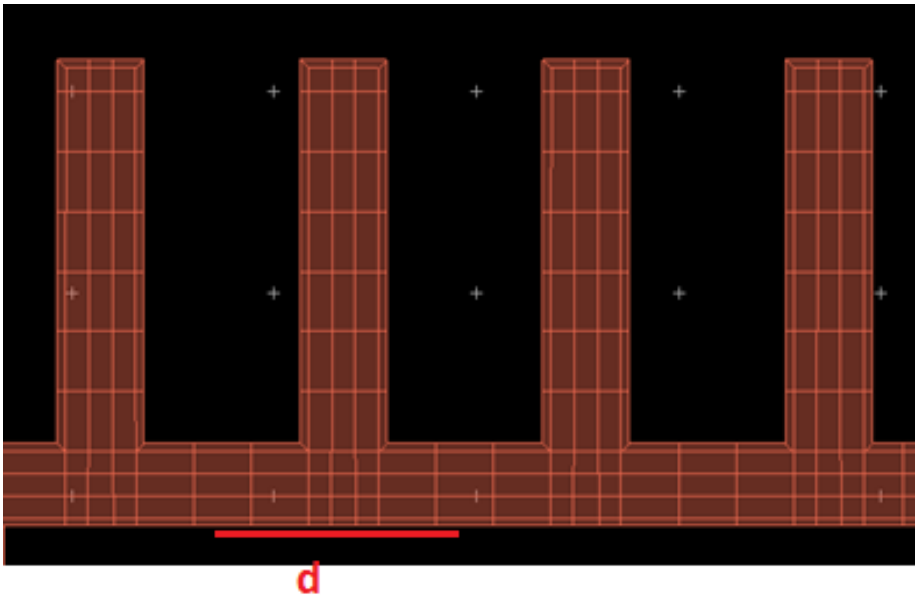


Figure 5.4: Layout of the second ATL design on ADS.

A different structure of ATL is shown on Figure 5.4. This structure consists of a thin transmission line with repeated capacitive stubs which effectively creates a series of high and low impedance lines [6]. Changing the parameters of the ATL allows you to get different electrical characteristics and physical dimensions. The formulas for the ATL are given below [7]:

$$C_p = \frac{\phi_{\text{ATL}}\left(Z_{o\text{TL}}^2 - Z_{o\text{ATL}}^2\right)}{N\omega_o Z_{o\text{TL}}^2 Z_{o\text{ATL}}} \tag{5.1}$$

$$\omega_o C_p = \frac{1}{Z_{o\text{Stub}}} \tan\left(\frac{\omega_o}{v_{p\text{Stub}}}\ell\right) \tag{5.2}$$

$$d = \frac{Z_{o\text{ATL}}\phi_{\text{ATL}} v_{p\text{TL}}}{Z_{o\text{TL}} N\omega_o} \tag{5.3}$$

The formulas and other factors put some constraints on what you can do with the ATL. The ratio $\frac{Z_{o\text{ATL}}}{Z_{o\text{TL}}}$ roughly determines the level of miniaturization you can achieve relative to a regular transmission line. This means that making the transmission line thinner (and therefore making $Z_{o\text{TL}}$ higher) will yield a shorter structure. The first formula shows that doing this will require the capacitance of the stubs to increase. The second formula tells us that in order to get a higher stub capacitance, we need to either make the stubs thicker or longer. The third formula gives the required per unit cell length. The variable 'N' is the total number of cells. There are also additional constraints such as how thin your PCB fab house can make the transmission lines and that the spacing between the capacitive stubs need to be at least $3h$ from each other, where h is the substrate height of your board. The reason for this limit on the spacing between stubs is to reduce crosstalk. The thinner your board, the more compact the structure will be because the stubs are allowed to be closer together.

This structure of the ATL was used in order to create the 4 components needed to make the Butler matrix.

5.3 Quadrature Hybrid

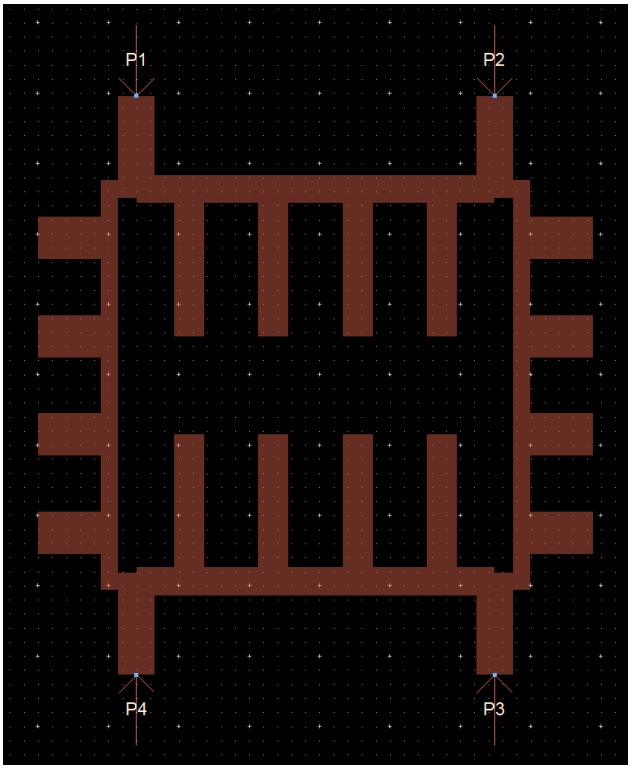


Figure 5.5: Layout of the quadrature hybrid using ATL.

Figure 5.5 shows the quadrature hybrid implemented using ATLs.

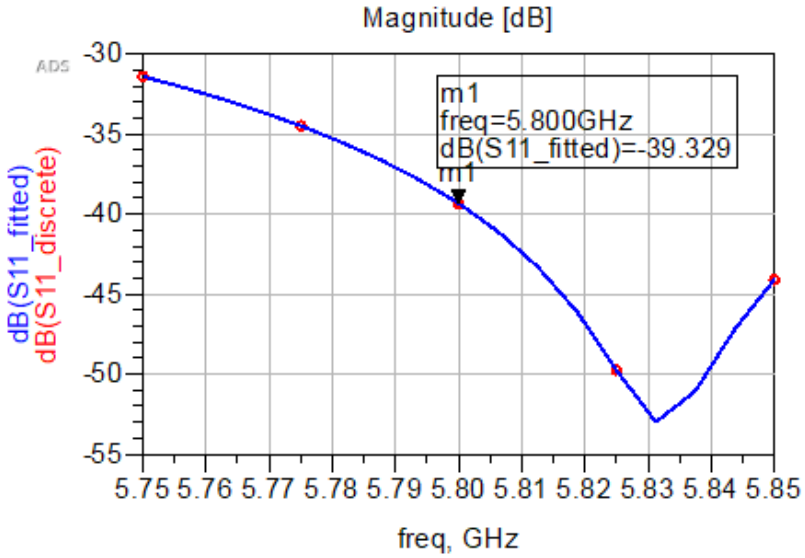


Figure 5.6: S_{11} parameter plot for the quadrature hybrid.

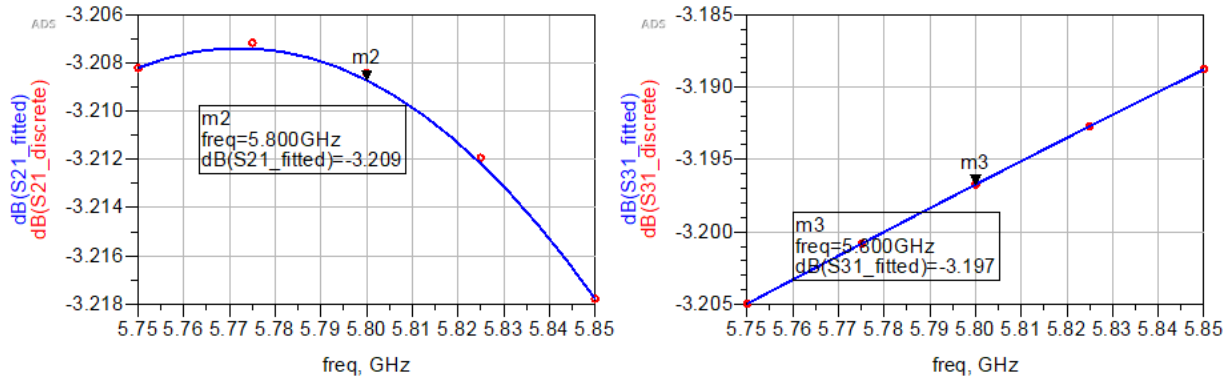


Figure 5.7: S_{21} and S_{31} parameter plots for the quadrature hybrid.

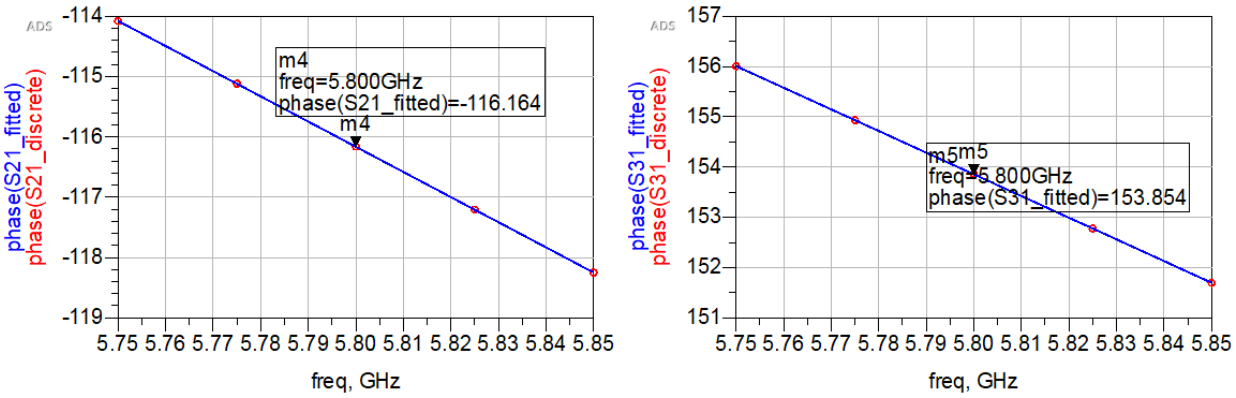


Figure 5.8: Phases of S_{21} and S_{31} for quadrature hybrid. One can see that there exists a phase difference between them.

The S-parameter plots presented in Figures 5.7 and 5.8 show that the quadrature hybrid has low reflection coefficient at port 1, nearly half of the power splitting between port 2 and port 3 equally and a phase difference of 89.982 degrees between port 2 and port 3. Ideally there should be -3 dB for S_{21} and S_{31} and a phase difference of 90 degrees between port 2 and port 3.

5.4 Crossover

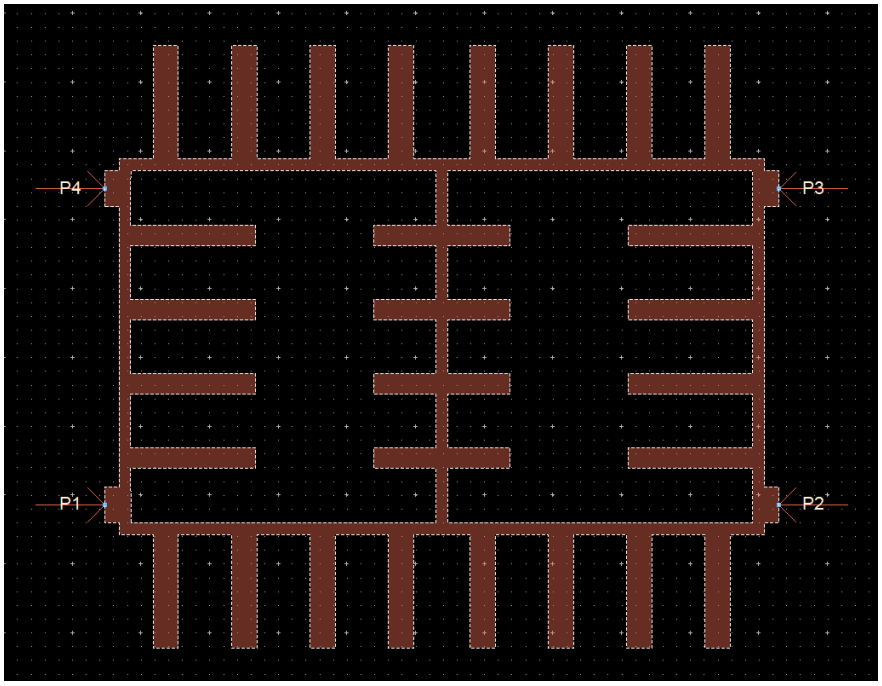


Figure 5.9: Crossover layout on ADS.

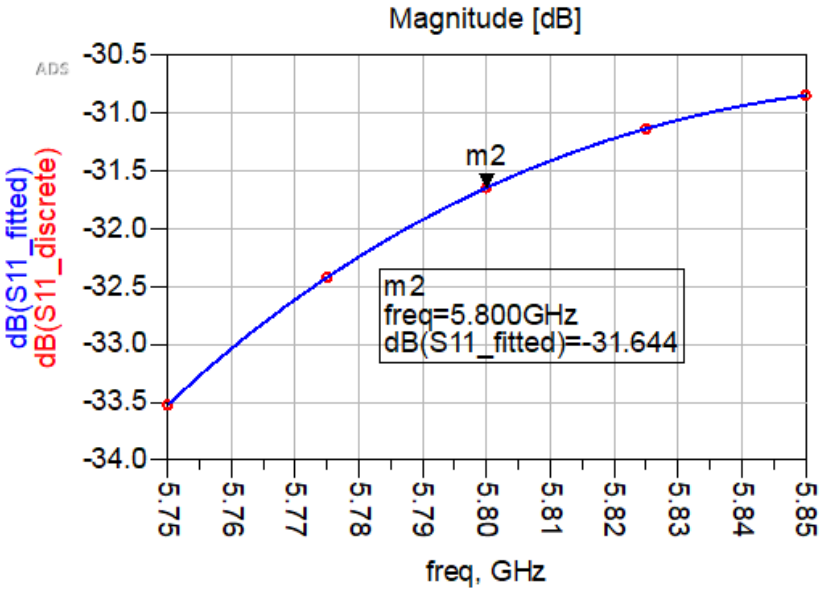


Figure 5.10: S_{11} plot for crossover

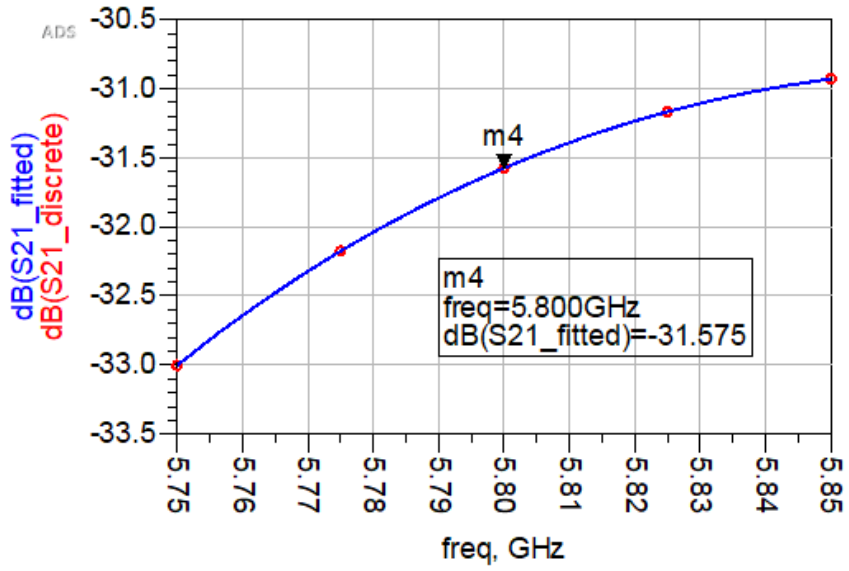


Figure 5.11: S_{21} plot for crossover

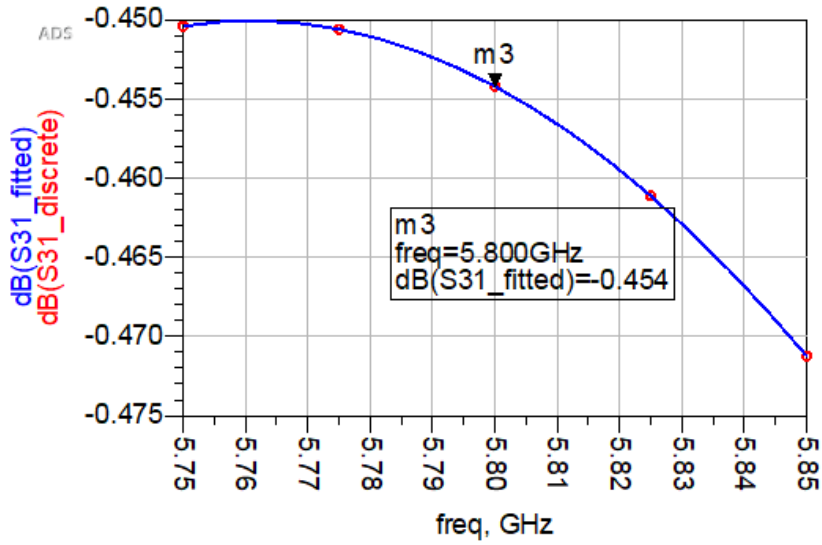


Figure 5.12: S_{31} plot for crossover

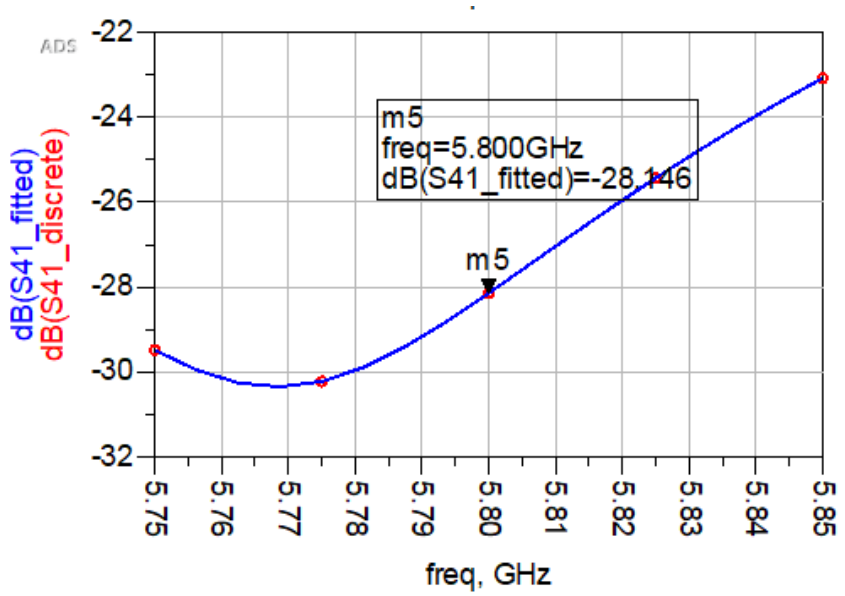


Figure 5.13: S_{41} plot for crossover

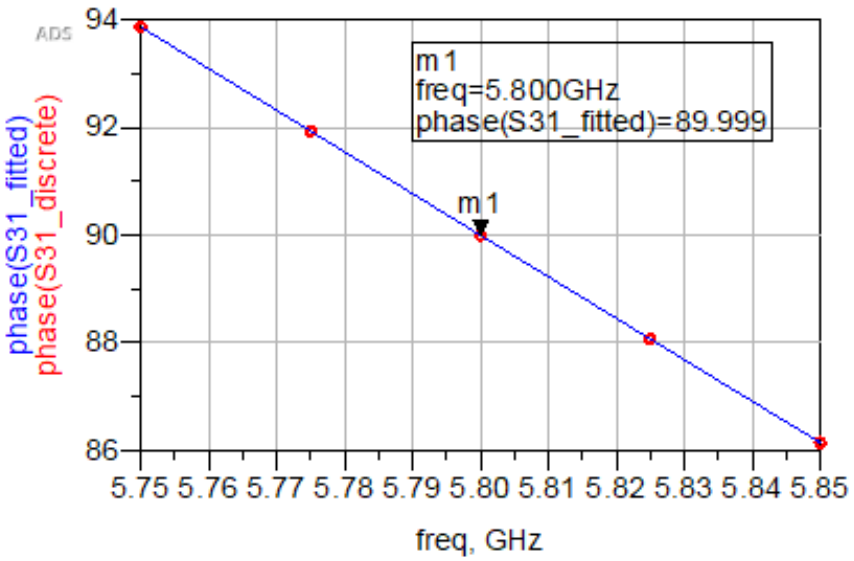


Figure 5.14: S_{31} phase plot for crossover

Figure 5.9 shows the layout of the crossover using ATLs. The S-parameter plots presented in Figures 5.13 and 5.14 show that most of the signal exits at port 3 when it enters at port 1 with very little signal going to the other ports or being reflected back. The phase difference between port 1 and port 3 is 270.001 degrees with the ideal value being 270 degrees.

5.5 45 Degree Phase Shifter

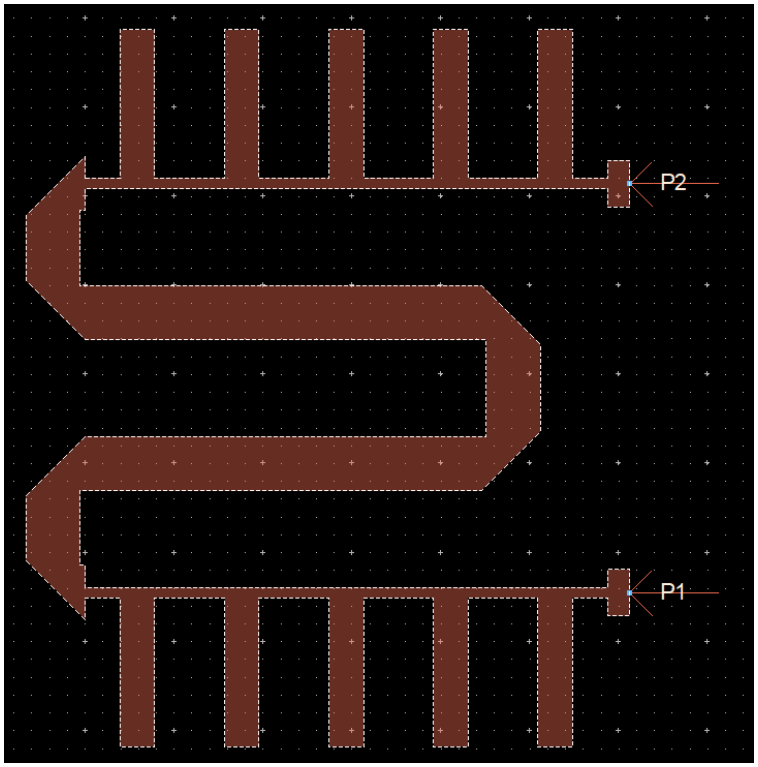


Figure 5.15: Layout of 45 degree phase shifter on ADS

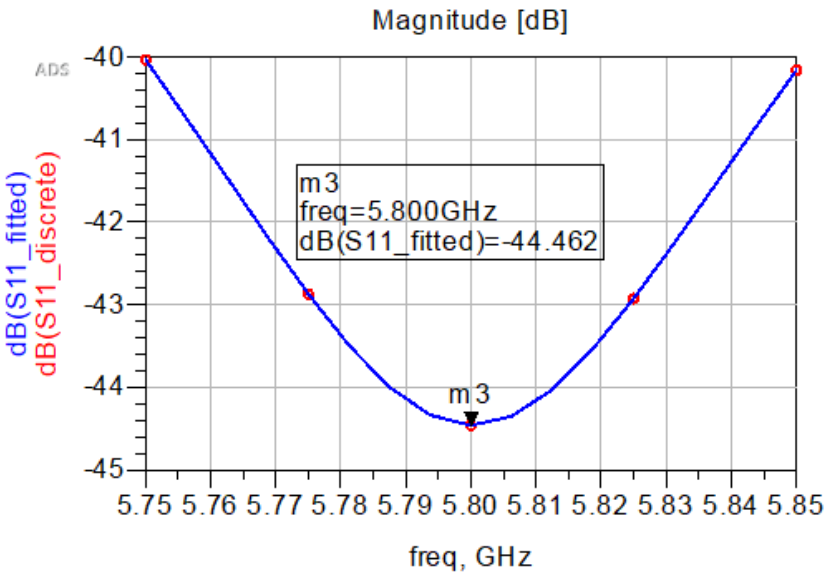


Figure 5.16: S_{11} plot of 45 degree phase shifter

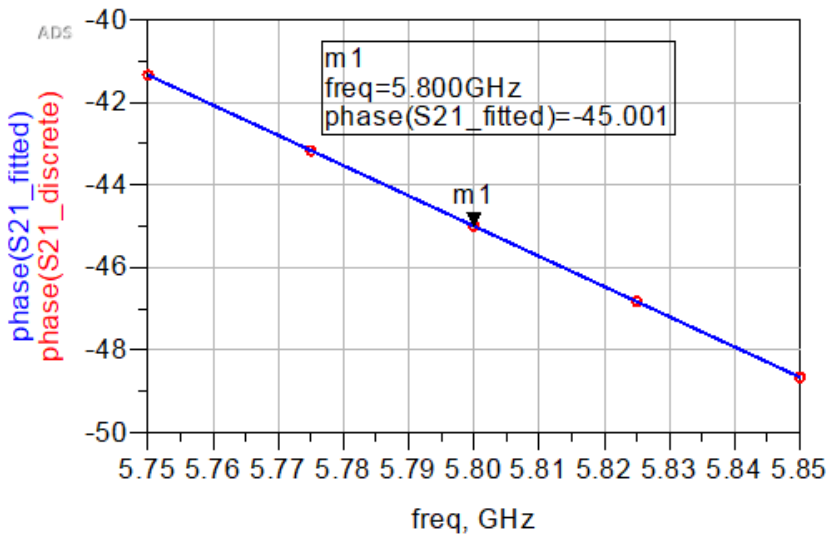


Figure 5.17: S_{21} phase plot of 45 degree phase shifter

Figure 5.15 shows the layout of the 45 degree phase shifter. The actual electrical length was made to be 360 + 45 = 405 degrees because a 45 degree phase shifter was too short to connect the components even with regular transmission line. This structure was made with a mix of ATL and regular transmission line. The reason for this was because meandering the lines makes more efficient use of area and ended up making the structure smaller. There is not enough space in the middle to use an ATL if a meandered line is used because of the stubs. The structure is resonant at 5.8 GHz with an S_{11} of −44.462 dB as shown in Figures 5.16 and 5.17. The phase shift is 45.001 degrees.

5.6 Extra Length

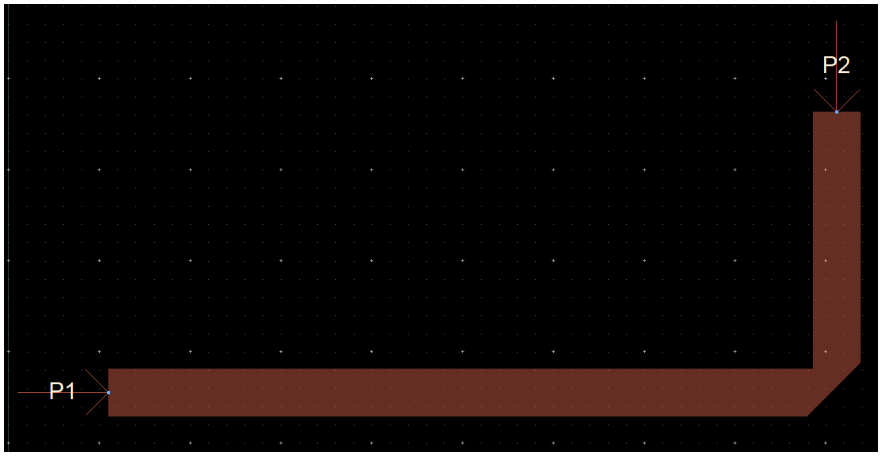


Figure 5.18: Layout of extra length on ADS which is used at the end of the butler matrix

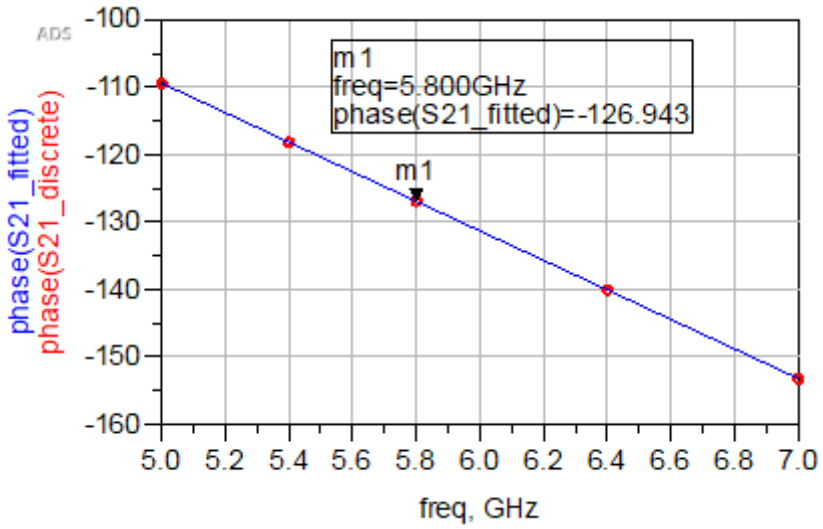


Figure 5.19: S_{21} phase plot of Extra Length

An extra length had to be introduced at the end of the butler matrix to make sure the patch antennas are spaced apart appropriately with $\frac{\lambda}{2}$ spacing, as shown in Figure 5.18. This introduces an extra 126.943 degree phase shift, as shown in the S_{21} phase plot (Figure 5.19).

5.7 90 Degree Phase Shifter

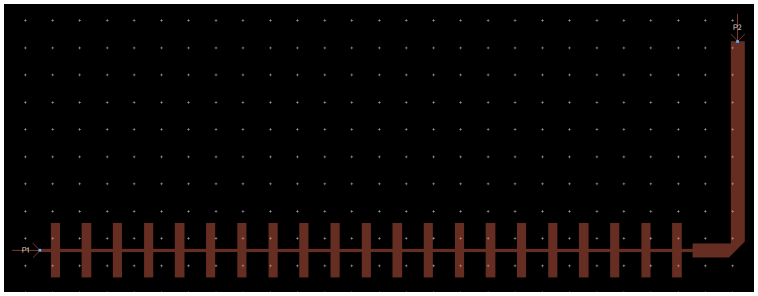


Figure 5.20: Layout of 90 degree phase shifter on ADS

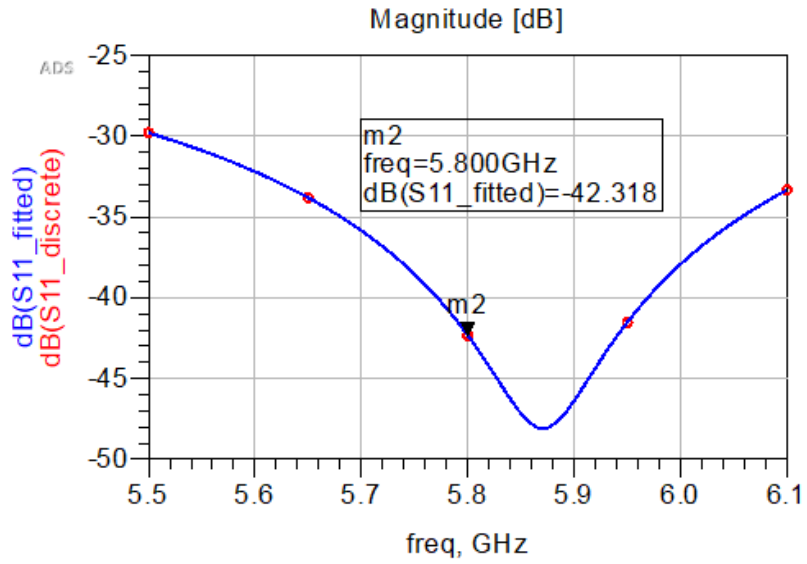


Figure 5.21: S_{11} plot of 90 degree phase shifter

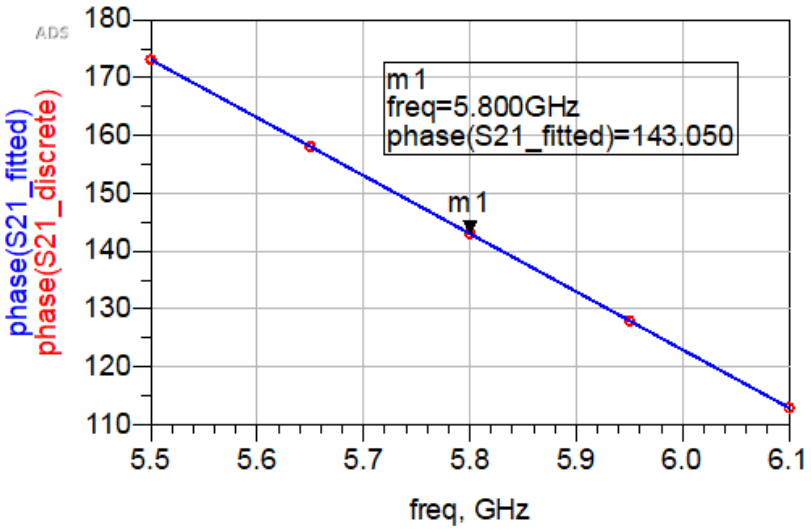


Figure 5.22: S_{21} phase plot of 90 degree phase shifter

The 90 degree phase shifter (Figure 5.20) is also too short to make with a regular transmission line. There needs to be a 360 degree phase shift added to it plus an extra phase shift of 126.943 degrees caused by the extra length. The total phase shift this structure needs to be is 576.943 degrees. The simulation results show that the phase shift is actually 576.95 degrees which is close to the ideal value, as shown in the S_{21} phase plot (Figure 5.22). The phase lag in ADS starts with 0, goes down to -180 and then wraps around starting from $+180$.

5.8 Whole Butler Matrix

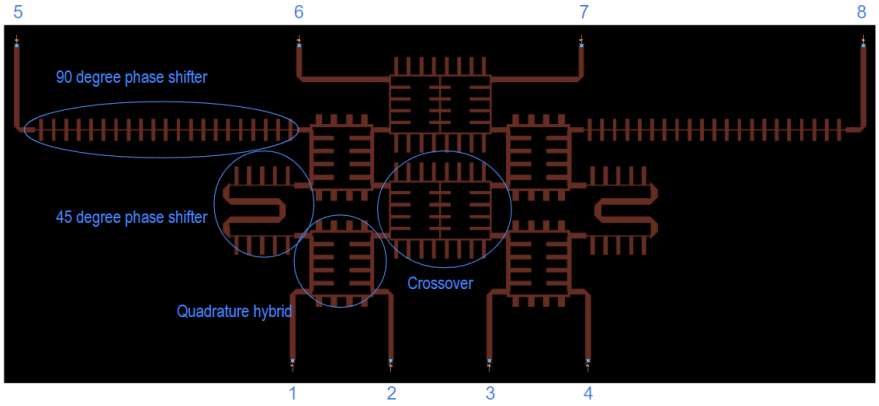


Figure 5.23: Layout of the whole butler matrix on ADS

Figure 5.23 shows the layout of the whole butler matrix. The ports 1-4 are the input ports and ports 5-8 are the output ports. The parts circled in blue are the 4 components used to build the butler matrix mentioned earlier. Below are some of the S-parameter plots for the Butler matrix. The values for S_{51} and S_{61} are similar to each other and quite close to the ideal value of -6 dB. The power splitting is quite balanced with almost $\frac{1}{4}$ of the power going to each output port. The phase at port 6 leads by 131.833 degrees compared to port 5. In other words, the phase at port 6 is -131.833 degrees that of port 5. The ideal value for the phase difference at the output ports when looking from input port 1 is -135 degrees. The complete S-parameter plots are shown in the appendix, and the only plots important to this discussion are shown here in Figure 5.24 up to 5.27. The summary of the S-parameter values and differential phases at the design frequency of 5.8 GHz for each port excitation are tabulated in Table 5.1 up to 5.4. The results show that the butler matrix works well in simulation since the power splitting are all quite equal and the phase differences are near the ideal values.

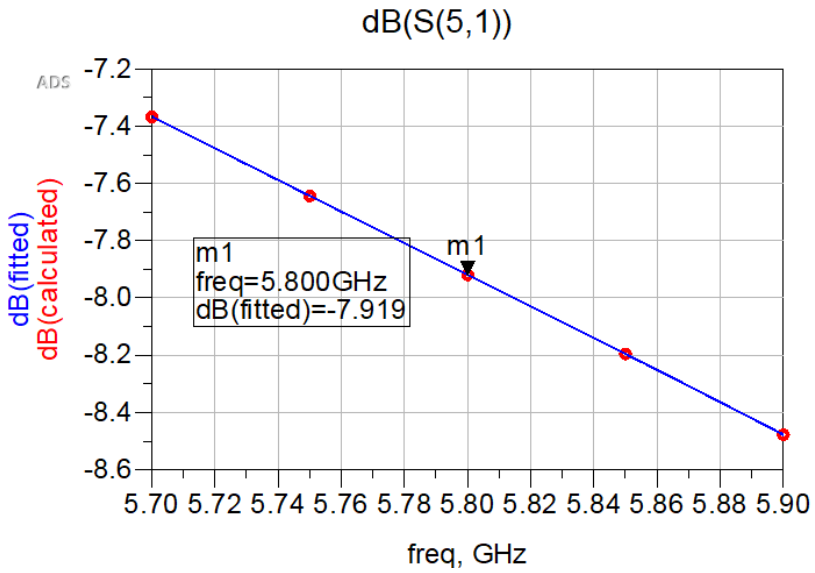


Figure 5.24: S_{51} plot of whole Butler matrix

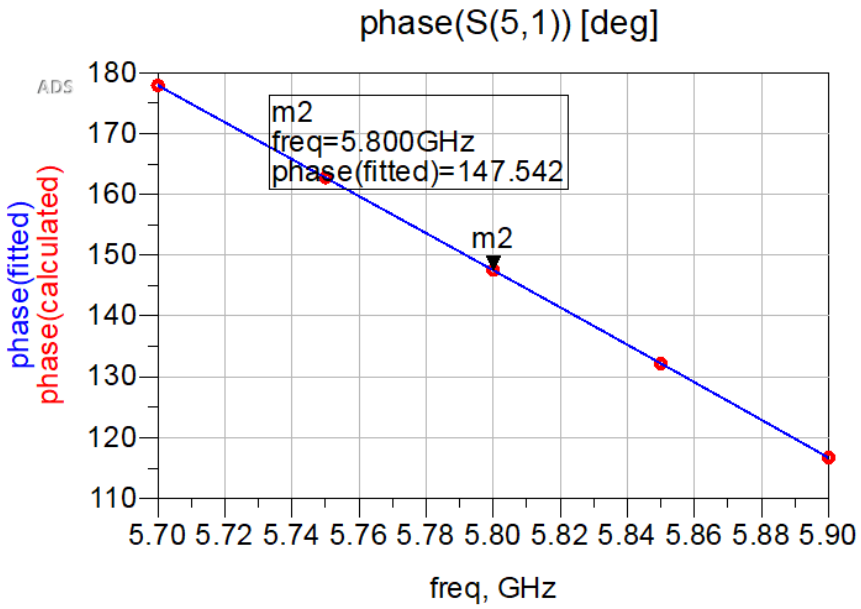


Figure 5.25: S_{51} phase plot of whole Butler matrix

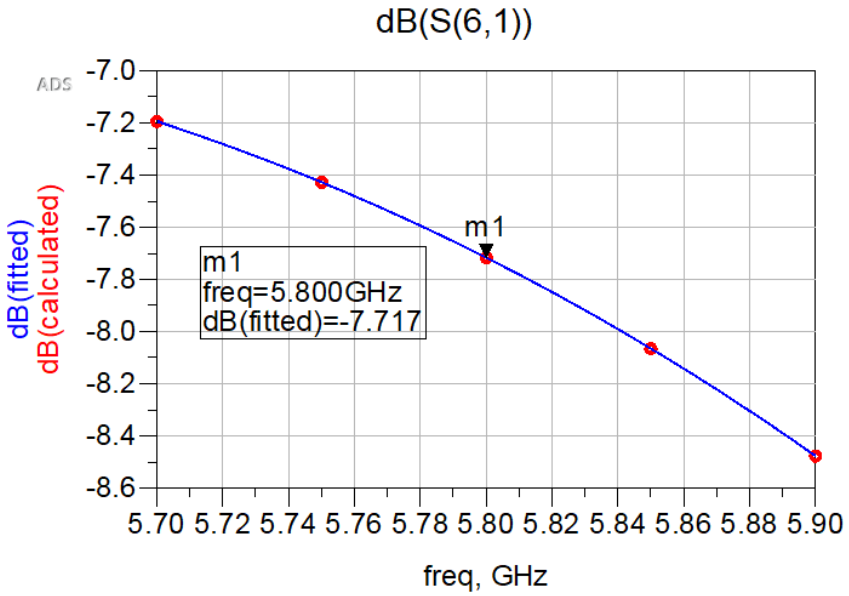


Figure 5.26: S_{61} plot of whole Butler matrix

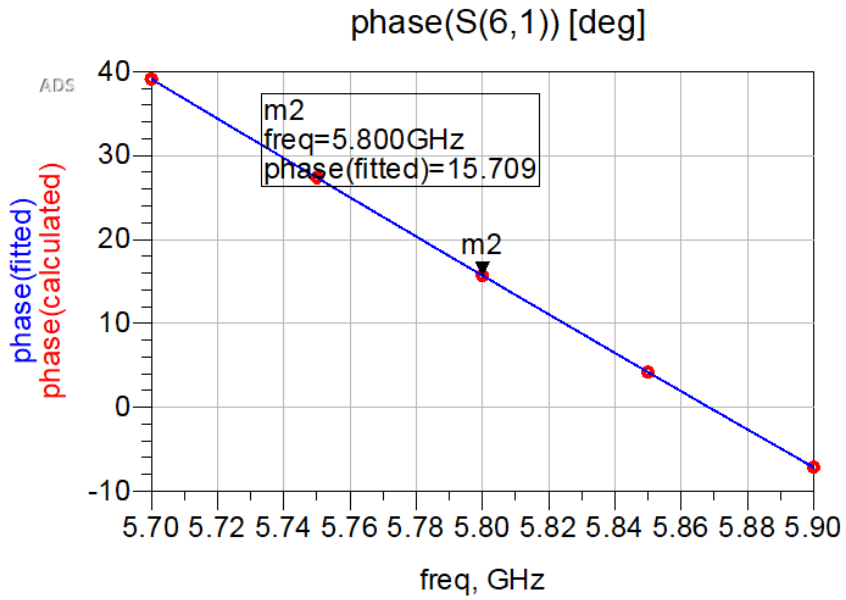


Figure 5.27: S_{61} phase plot of whole Butler matrix

S-Parameter	***Power (dB)***	***Phase shown on plot (degrees)***	***Phase difference (degrees)***
S_{51}	−7.919	147.542	N/A
S_{61}	−7.717	15.709	−131.833
S_{71}	−6.426	−120.055	−135.764
S_{81}	−7.53	101.859	−138.086

Table 5.1: S-parameters of outputs with respect to port 1. Note: Ideal phase difference is −135 degrees.

S-Parameter	***Power (dB)***	***Phase shown on plot (degrees)***	***Phase difference (degrees)***
S_{52}	−6.923	59.68	N/A
S_{62}	−7.717	98.696	39.016
S_{72}	−6.426	146.324	47.628
S_{82}	−7.53	−167.13	46.546

Table 5.2: S-parameters of outputs with respect to port 2. Note: Ideal phase difference is 45 degrees.

S-Parameter	***Power (dB)***	***Phase shown on plot (degrees)***	***Phase difference (degrees)***
S_{53}	−7.543	−167.09	N/A
S_{63}	−8.675	146.316	−46.594
S_{73}	−7.221	98.741	−47.575
S_{83}	−6.922	59.684	−39.057

Table 5.3: S-parameters of outputs with respect to port 3. Note: Ideal phase difference is −45 degrees.

S-Parameter	***Power (dB)***	***Phase shown on plot (degrees)***	***Phase difference (degrees)***
S_{54}	−7.53	101.897	N/A
S_{64}	−6.427	−120.059	138.044
S_{74}	−7.717	15.754	138.044
S_{84}	−7.919	147.54	131.786

Table 5.4: S-parameters of outputs with respect to port 4. Note: Ideal phase difference is 135 degrees.

6 System Evaluation

The senior design objectives were accomplished by using the hub provided from last year's. The list of components used to accomplish the goals of this senior design project are shown below.

Item Description	***Amount***
First batch of antennae	$806.46
RF cables and connector	$217.70
Power indicator boards	$287.50
1.1 kΩ resistors	$13.21
Surface mount LEDs	$15.21
300 Ω and 3.3 kΩ resistors	$287.50
Comparators & resistors for breadboard	$68.04
Through-hole LEDs	$12.65
Headers, resistors, and comparators for PCB	$232.58

Table 6.1: Table of components used in our senior design project. Total cost is $1665.58.

For this year's project, the results of the simulation conducted for a miniaturized hub as reported in Chapter 5 were very promising and deemed suitable for paper publication. Therefore, for our personal interest to extend the work, an extra prototype was fabricated as shown in Fig 6.4. This is now an integral part of our system.

6.1 Test Setup

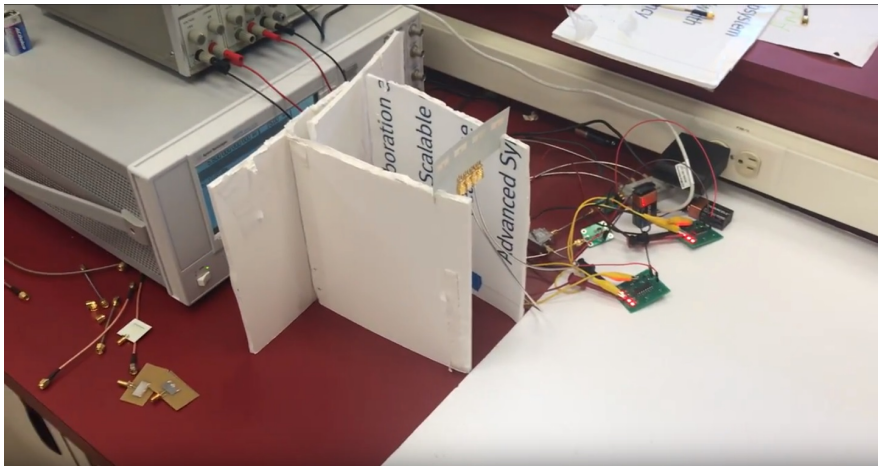


Figure 6.1: Setup of our hub.

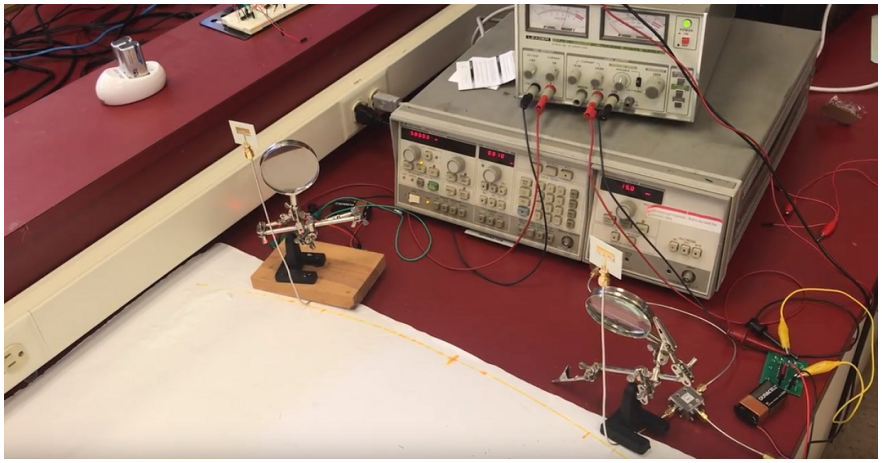


Figure 6.2: Setup of the user side.

Figures 6.1 and 6.2 show the 2 sides of our whole system which consists of the hub and the user end. We have done previous testing for the bidirectional link using the old butler matrix and patch antennas which are made by the previous senior design group. It was confirmed long ago that the bidirectional link was working. However, when paired with the power indicator, we saw that there was a relatively significant amount of power going through the wrong port in the RF circulator and then going into the power indicator. This acts as the "noise" in our system. Since this noise is too large relative to the signal being received from the other side, we could not have the signal generators to be on at the same time for the user and hub if we wanted a bi-directional link.

6.2 Link budget calculation

The Friis transmission equation [1] shows how much power is being transmitted to the other side of the system (in this case, from the hub to the user end).

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi R)^2} \tag{6.1}$$

P_t is 15 dBm for our system. G_t is 4.163 dB which is the gain for the hub when ports 2 and 3 are excited. G_r is 4.9665 dB which is the gain for the patch antenna on the user side. R is 1 meter. λ is $\frac{3}{58}$ meters. The values for gain are based on simulation which will be more ideal than the actual fabricated components. P_r turns out to be -23.58 dBm. Measurements using the spectrum analyzer in lab say that the received power is around -30 dBm under the same conditions. This is about only $\frac{1}{4}$ of the power received as the ideal case using the Friis transmission equation. There are losses in the RF cables, RF switch, and RF circulator that is not yet accounted for. Another big issue is the low gain of the array of patch antennas on the hub side because of the thin boards and the fact that the S_{11} is around -3 dB at 5.8 GHz meaning that half of the power is being reflected back from the antenna.

It is difficult to try to extend the range beyond 1 meter because +15 dBm is almost the highest power the signal generator can output already and only 2 lights turn on at the user side (out of 4 lights). We were able to get only 1 light showing at a range of 1.88 meters. This is the maximum range where our system still works reliably.

The old hub and new hub have similar performance in terms of power reaching the other side. They are within 1 dB of each other. This meets one of our objectives.

6.3 Results

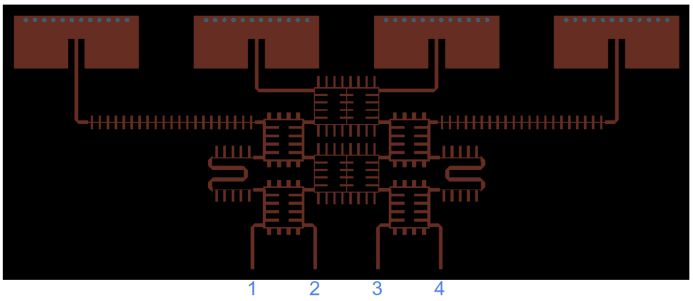


Figure 6.3: Layout of Butler matrix and modified patch antennas that make up the hub

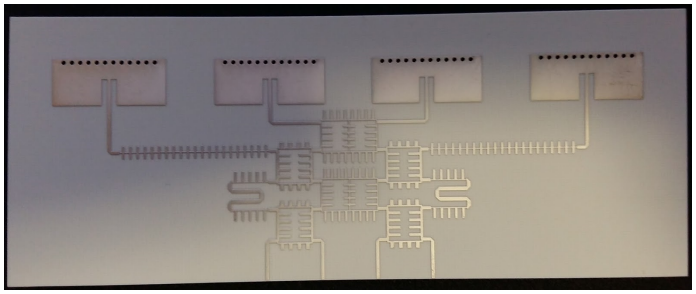


Figure 6.4: Fabricated Hub

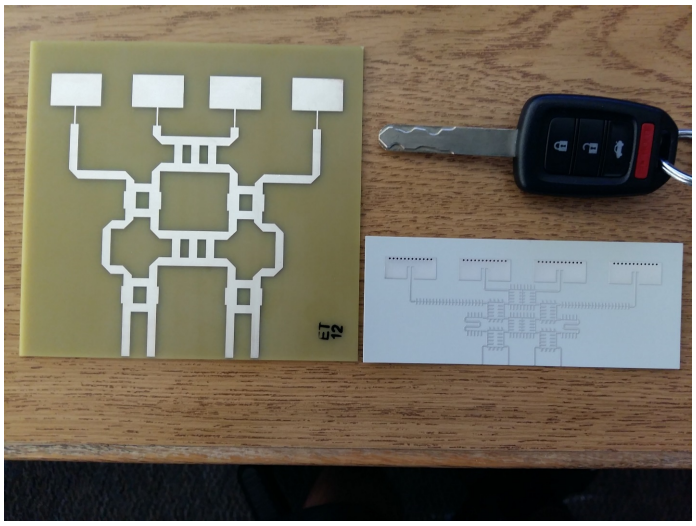


Figure 6.5: Size comparison between old (left) and new hub (right)

The Butler matrix is combined with the quarter wave patch antenna to make the hub. The patch antennas had to be modified to work for a board thickness that is 3 times thinner compared to the first version of the patch antenna. This time it was made using ADS. It turns out that using this new board thickness caused the inductive effect of the via to decrease so the positive imaginary impedance seen at the input of the antennas is also decreased. As a result, there was no need to put a microstrip gap as a capacitor. The S-parameters for the simulation and actual measurement can be found in the appendix. The S-parameters are not that critical to the performance of the Butler matrix as long as not too much power is reflected back which is indeed the case for simulation and measured results. The comparison picture shows that the new phased array antenna is about $\frac{1}{3}$ of the old board's area. The results for the modified patch antenna and the entire hub are shown in the figures below.

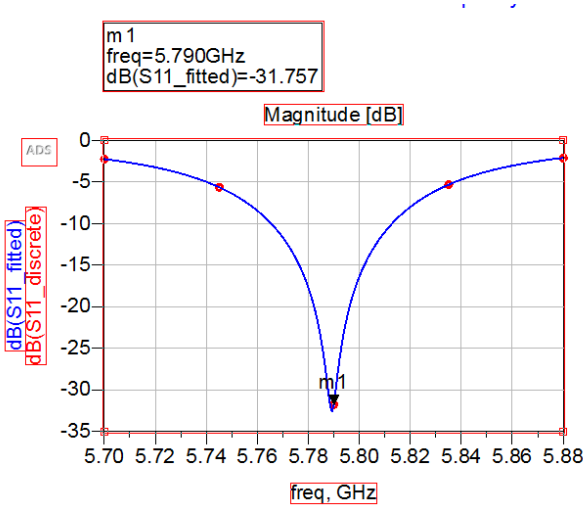


Figure 6.6: S_{11} plot of the modified patch antenna on ADS

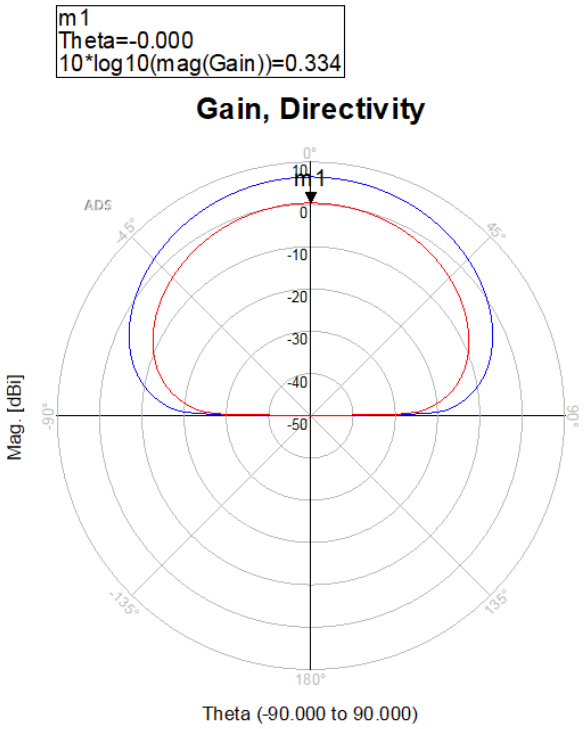


Figure 6.7: Pattern plot of the modified patch antenna on ADS

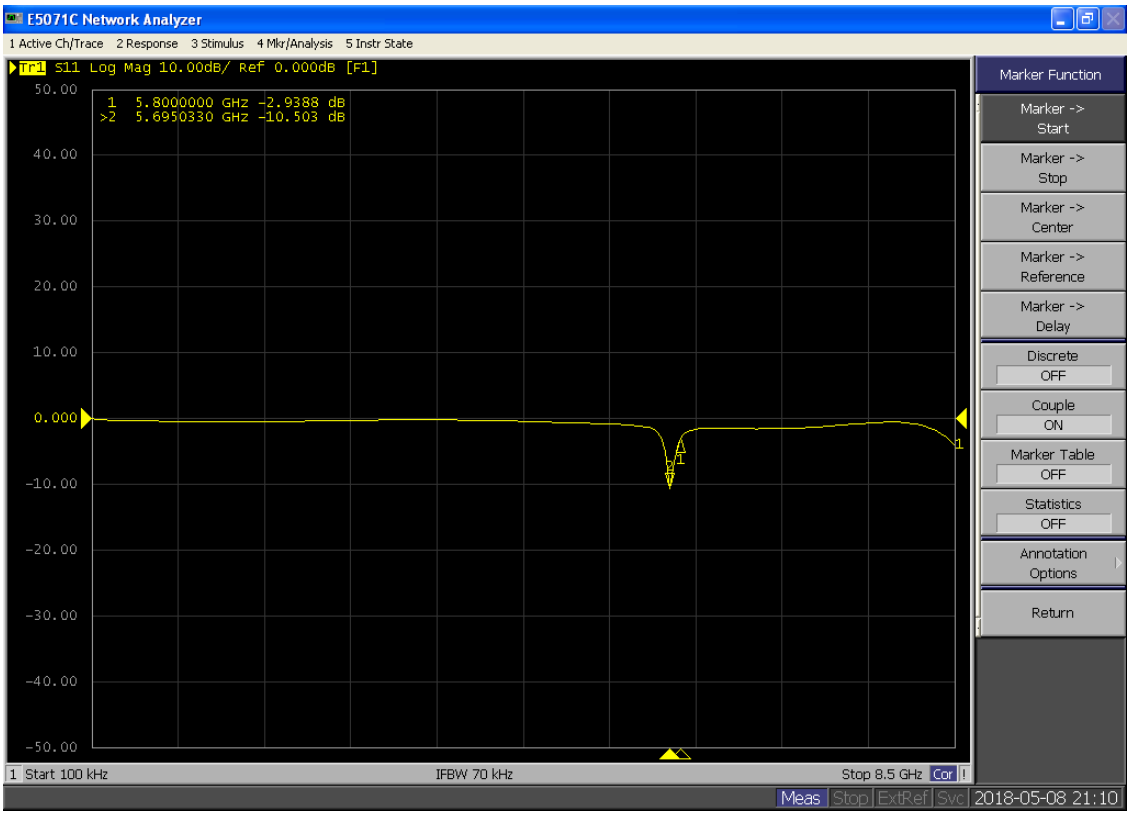


Figure 6.8: S_{11} plot of the modified patch antenna on VNA

The simulation result for S_{11} is good but the actual S_{11} plot turns out to have bad performance. The center frequency changed from 5.79 GHz to 5.7 GHz. Even though this is not considered a big change, the patch antenna is a resonant antenna and has a very narrow fractional bandwidth. The S_{11} turns out to be -3 dB at 5.8 GHz on the actual measured results for a single patch antenna. This is problematic because the antenna itself already has a low gain of 0.334 dB. A bad S_{11} performance will cause the realized gain to drop even further. There is a paper that shows that reducing the board thickness after a certain point will reduce the gain of a patch antenna significantly [8].

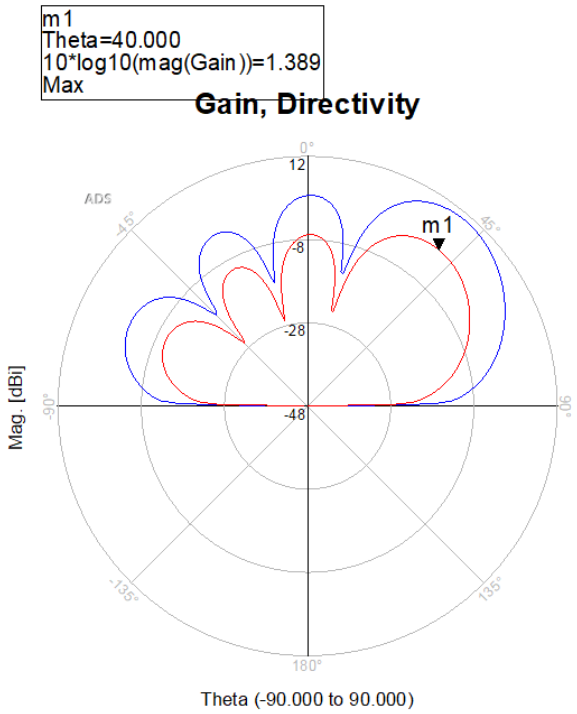


Figure 6.9: Pattern plot of hub with port 1 excited

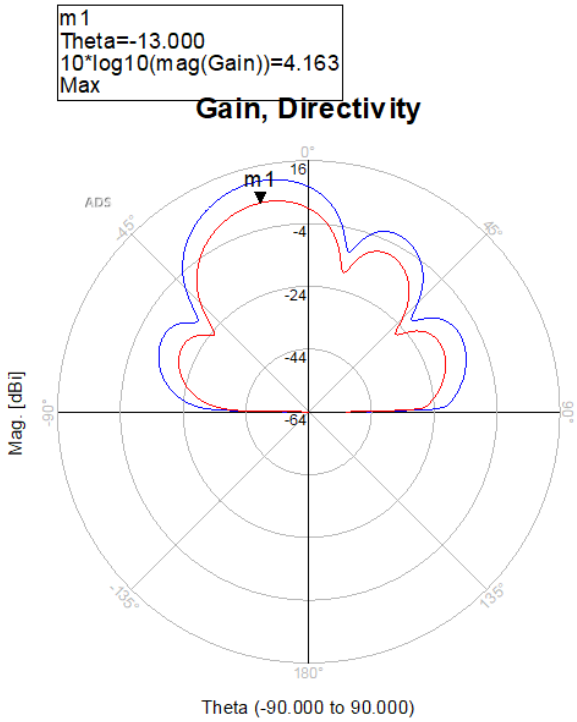


Figure 6.10: Pattern plot of hub with port 2 excited

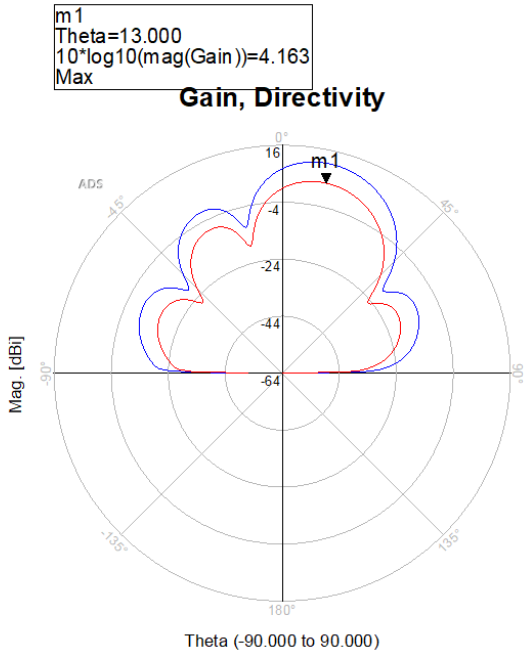


Figure 6.11: Pattern plot of hub with port 3 excited

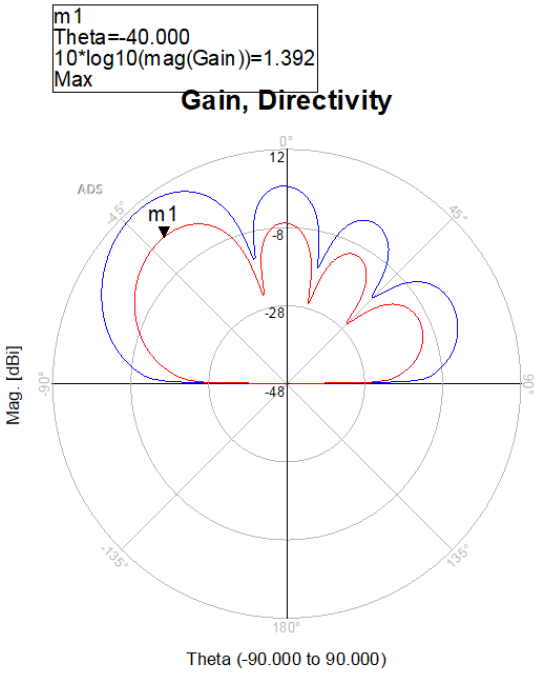


Figure 6.12: Pattern plot of hub with port 4 excited

The pattern plots for the various port excitations as presented in Figures 6.9 through 6.12 show that the beamswitching works. Different port excitations clearly direct the main lobe to different angles. Ports 1 and 4 direct the main lobe to 40 degrees from the center while ports 2 and 3 direct the main lobe to 13 degrees from the center. There are some side lobes but they are much smaller in power than the main lobe. Keep in mind that the pattern plots are in dB so the side lobes look big when they are actually only a fraction of the main lobes power. Another observation is that ports 2 and 3 work much better than ports 1 and 4. The gain is larger and the side lobe levels are lower.

7 Core Requirements

7.1 Environmental Sustainability

There are a few things we need in order to create the different components used in our senior design project. We require the services of the PCB fab house and some pre-bought components. The materials used in this project are the hydrocarbons used in the making of the substrate of the the printed circuit boards (PCB), which may not be environmental friendly. The RF to DC converter that we use is also built on a PCB. Other components that are not made on PCB are the RF circulators which are made of ferromagnetic materials and coaxial cables.

All the components we use are non-biodegradable. PCBs also tend to consist mostly of the substrate which are non-metallic. The non-metallic parts dominates the PCB by weight and they are difficult to recycle. Only the metallic components are easy to recycle but they make only a small part of the PCB and still need to be sorted out from other different types of metals. Fortunately our PCBs are quite small in size.

Our senior design is a system built out of the many different components. Each individual components have a different expected duration of the product life. The RF circulators for example have an incredibly long life cycle and can be reused for other purposes. They are quite durable and reusable. The antennas that we make can also be reused for different purposes since our system is modular as long as the application is in the 5.8 GHz range (which there are many). Cables can also be detached from our system and used for other applications. Some of our components are less durable or built for a specific purpose. Those will be harder to reuse and have a shorter life cycle. The RF to DC converters are made cheaply and are physically fragile. The power indicator circuit is only used for a specific purpose. It shows a visual measure of the power received in our system. It has 4 light indicators and if you want more or less then youll need to make another one from scratch. The range of power that the power indicator circuits work with is also limited to our system. A significantly different system such as one that uses high power antennas or high distance transmission will need a different power indicator.

7.2 Social Sustainability

The product will benefit the users by allowing them to have access to mobile communication and give priority to users that need them the most. Some people need access to communication more than others or there are applications that demand urgent communication. The system intends to satisfy that need. Its easy to use since you can program the switch in order to use an algorithm that will best meet the objective (though our project doesnt deal with the programming aspect). There will be no negative effects on welfare as it will only benefit the users in getting more access to communication, and there may be negative impact on health due to RF radiation, but research does not have conclusive evidence that RF radiation does negatively impact the peoples health at this frequency.

7.3 Economic Sustainability

The power indicator will provide economic stability because it is simple and cheap; the number of components involved is pretty few, and they are very simple. It will have all of the necessary components for its purpose and it uses the necessary resources efficiently. Other components like FPGAs and microcontrollers like arduinos can also be used in order to provide the same functionality. However, they are general purpose devices and thus have a lot of other components are are unused and unnecessary. This drives up cost especially when looking from the point of view of mass production.

Some components such as the RF circulators are not economically viable; the circulators cost $150 each. 1 RF circulator is needed for every user and ideally 4 is needed at the hub. Unfortunately we have not found a way to get around this if we still want the same functionality. A couple of the RF-related PCBs also use a Rogers RO4350B substrate which are substantially more costly than FR4 epoxy (which can be used for the power indicator and other lower fre-

quency applications). This might not be viable for mass production. It is mostly used for specialized components or equipment and prototype boards in order to get reliable results. Using a higher end and lower dielectric FR4 family of substrates will be more suitable for mass producing the antenna circuits.

7.4 Ethics

What we plan to do with our senior design is to help develop internet infrastructure with a low cost and portable solution in place. The solution will already have a comprehensive working system in place that can send and receive data simultaneously. This is particularly useful in developing nations, especially in rural areas. Over 60% of people (mostly from developing countries) still lack internet connectivity. We will have a beamforming network in place that is able to switch the angle of the main lobe of the beam. This means that we can give more priority to people who need the system most by having the beam forming network direct the main lobe to them longer compared to others who need less data.

A good engineer should be able to learn new necessary things for a certain project. For example, one of the engineers should learn a bit of RF and communications for this project just enough to understand what the other person is doing in a general sense. The engineer should also be able to learn new things on his/her own field to advance themselves with practical experience. A good engineer should also identify and consider the side effects of working on the project. Side effects such as health and environmental impacts, economic impacts and social impacts. Examples specific to our project would be the environmental impacts of manufacturing the antennas and beamforming network or the side effects of exposing people to electromagnetic fields at 5.8 GHz.

By making the uplink system wireless, we plan to reduce labor costs (and costs in general) of setting up the system especially for those who are living on rugged terrains. We also hope to design them so that it will have very minimal impact on human health since RF waves may be a concern on human health. We will also make it so that the system does not intrude on peoples privacy or collect their data.

7.5 Artwork

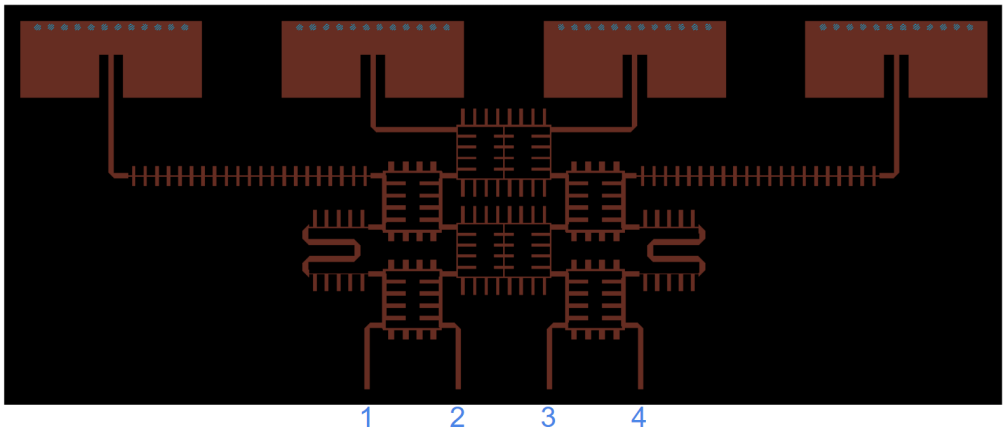


Figure 7.1: Submission for artwork requirement for Brian Tjahjadi

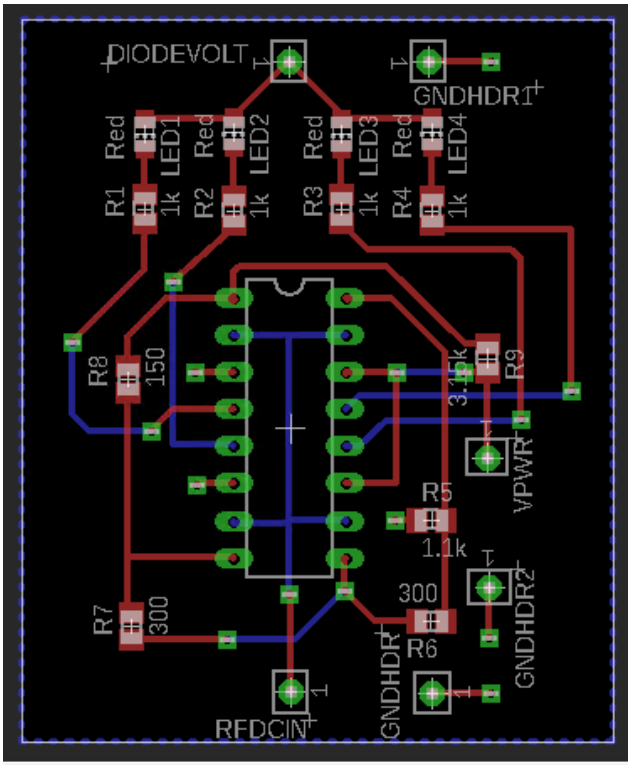


Figure 7.2: Submission for artwork requirement for Andrew Song

8 Conclusion

8.1 Analysis of Objectives Satisfied

We have accomplished most of the original objectives. We were able to implement downlink and uplink capability. The power indicator is able to display signal reception with 4 LEDs without the use of a microcontroller. The patch antennas were able to be miniaturized successfully. Additionally, the butler matrix was also miniaturized which reduced the size of our system even further. The performance of the user side antenna met the objectives of having a larger gain than 3 dB and smaller S_{11} than -10 dB. However, the array of patch antennas used at the hub did not meet these two specifications. It still worked well enough for the whole system to work though.

8.2 Timeline of Project

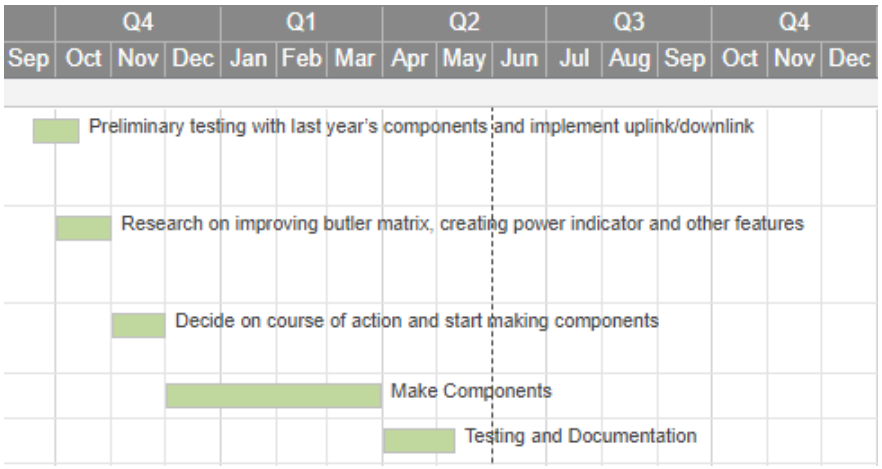


Figure 8.1: Expected timeline on Gantt chart.

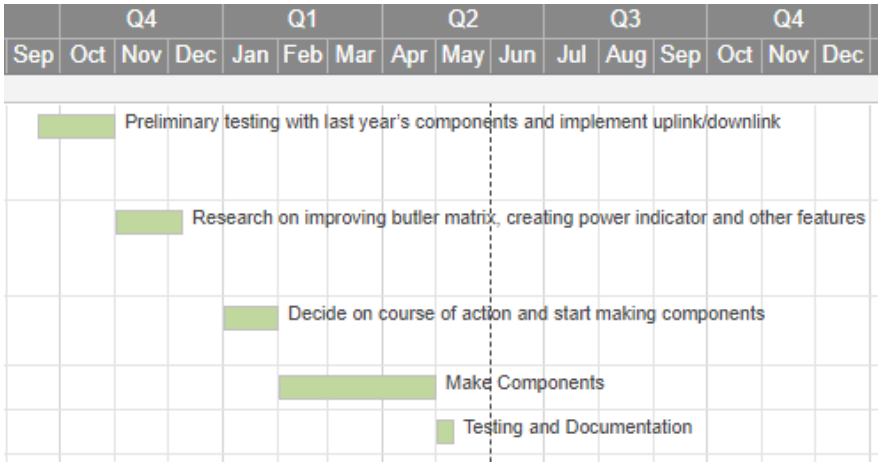


Figure 8.2: Actual timeline on Gantt chart.

9 Appendix

9.1 Butler Matrix S-parameters

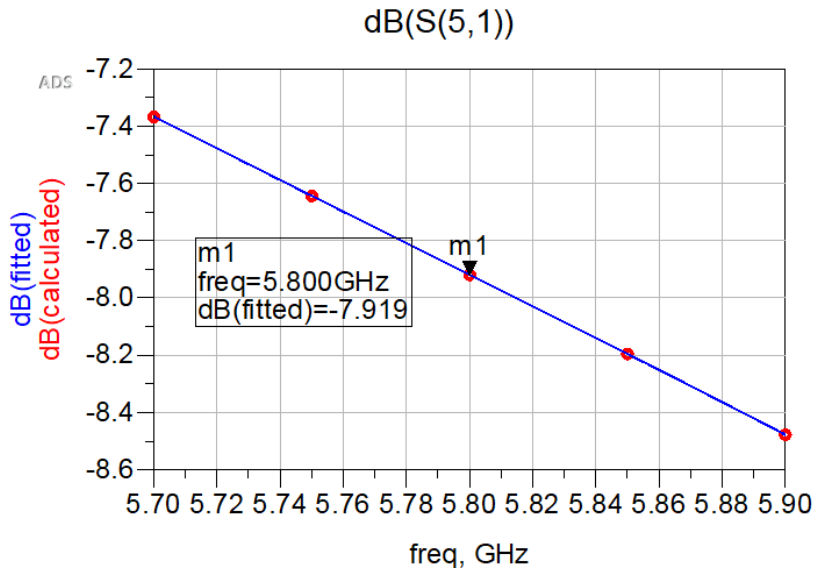


Figure 9.1: S_{51} plot of the Butler matrix.

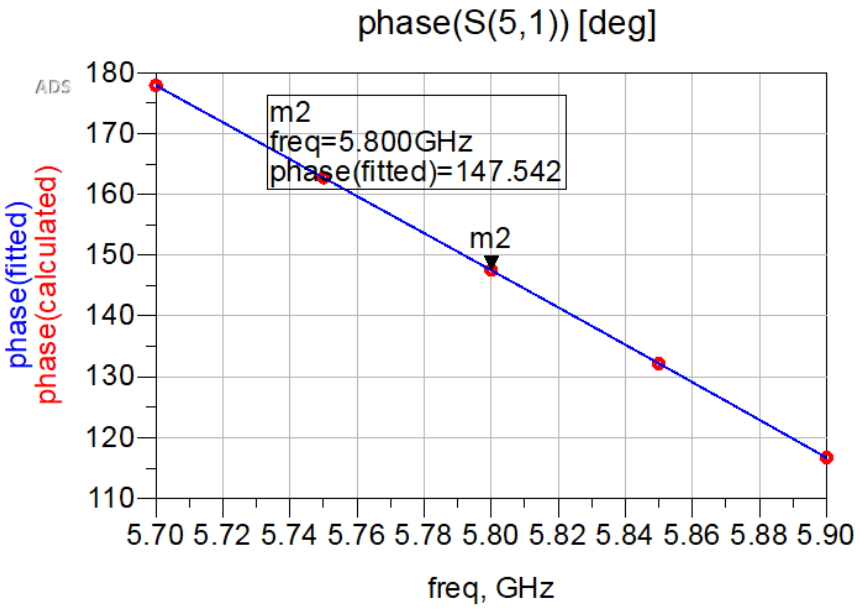


Figure 9.2: S_{51} phase plot of the Butler matrix.

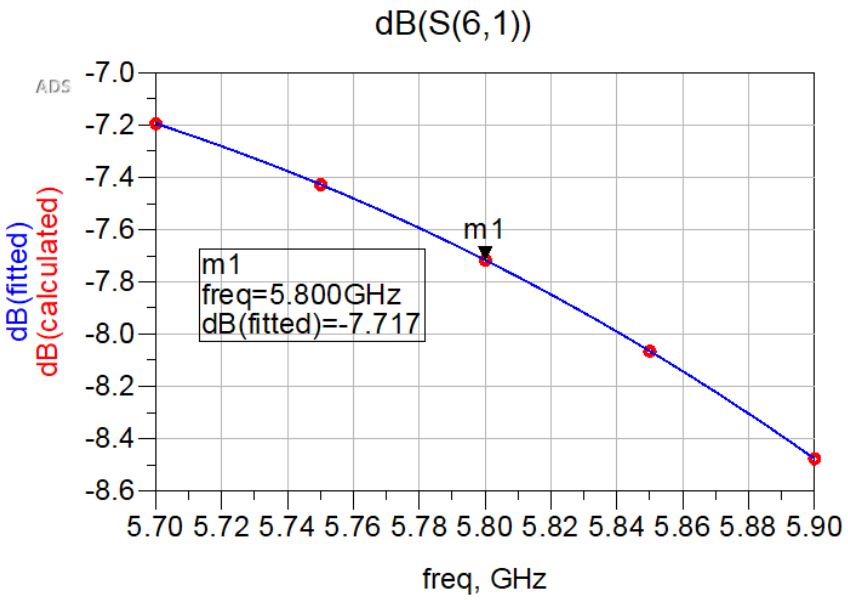


Figure 9.3: S_{61} plot of the Butler matrix.

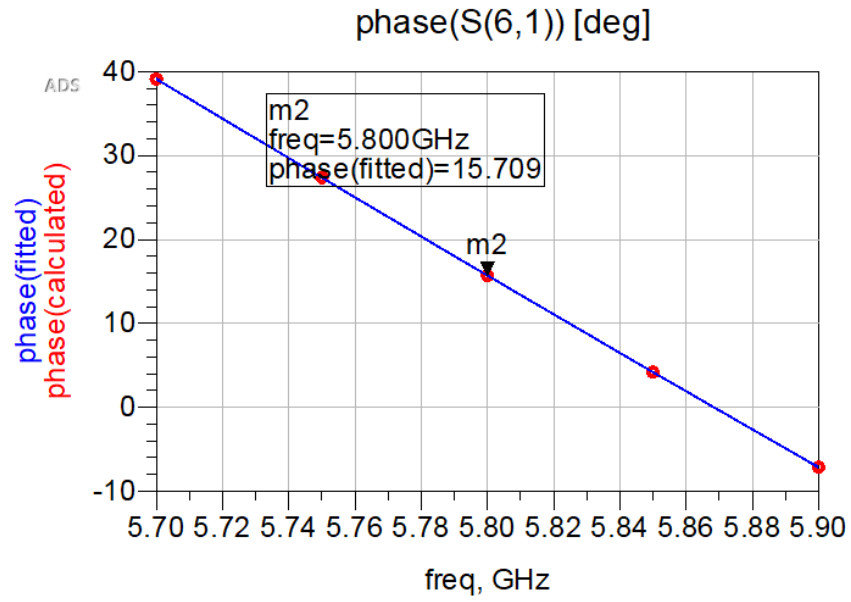


Figure 9.4: S_{61} phase plot of the Butler matrix.

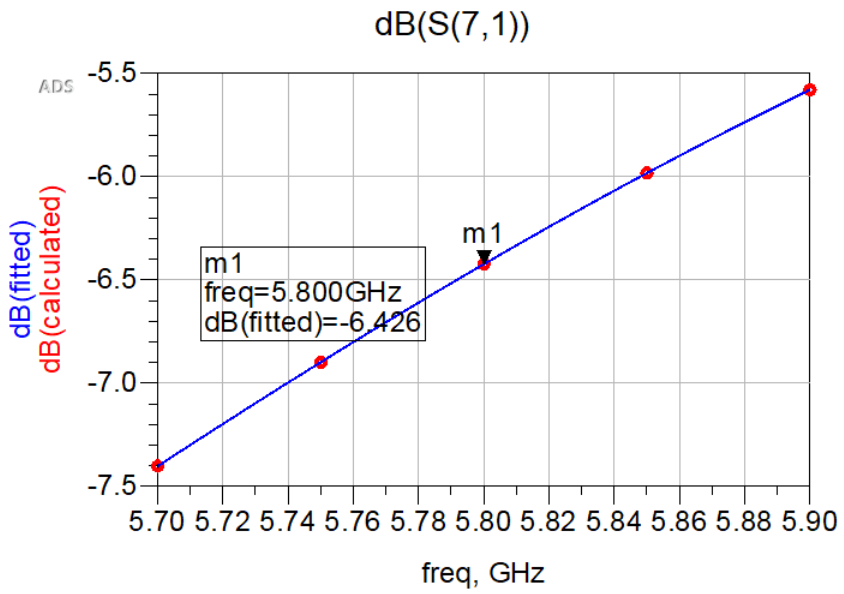


Figure 9.5: S_{71} plot of the Butler matrix.

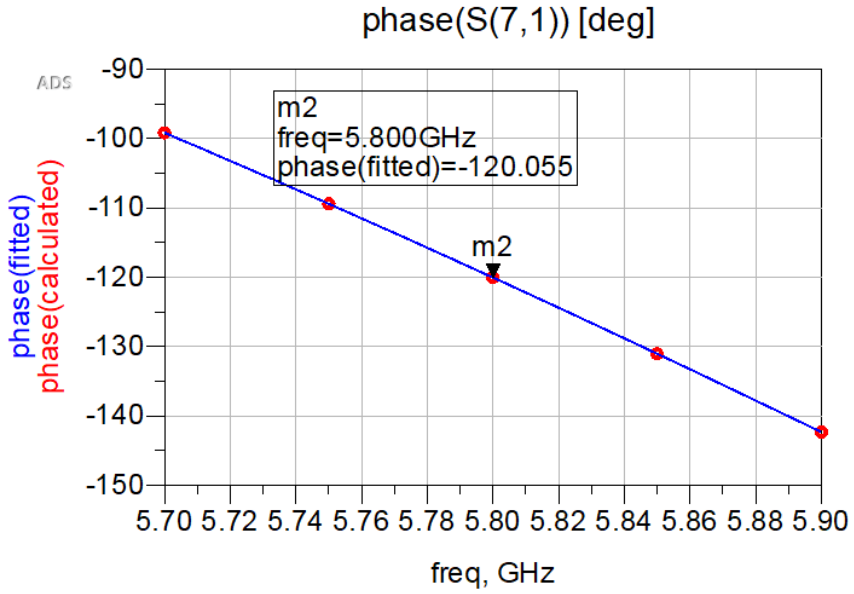


Figure 9.6: S_{71} phase plot of the Butler matrix.

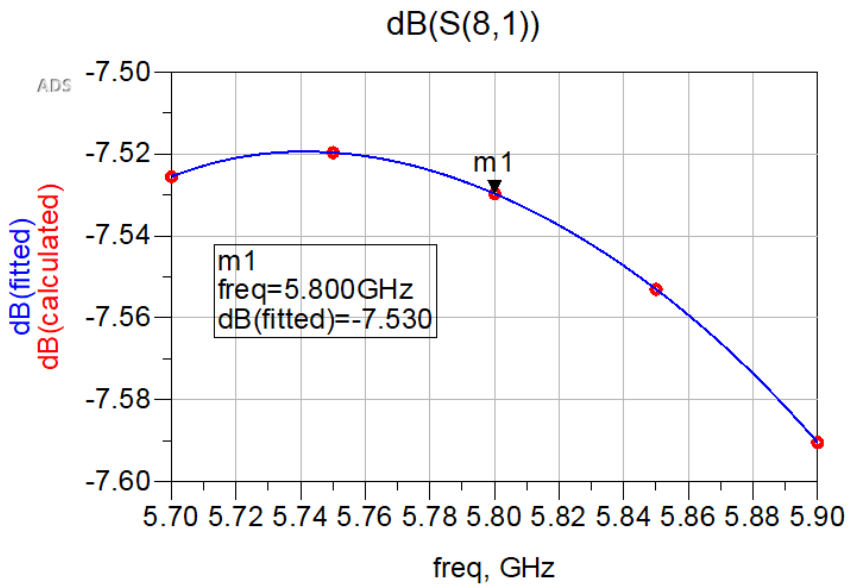


Figure 9.7: S_{81} plot of the Butler matrix.

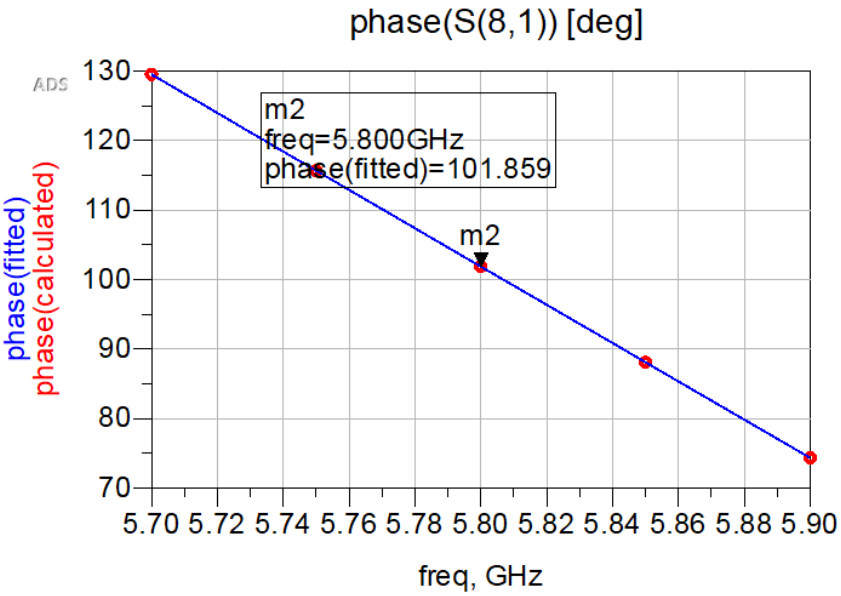


Figure 9.8: S_{81} phase plot of the Butler matrix.

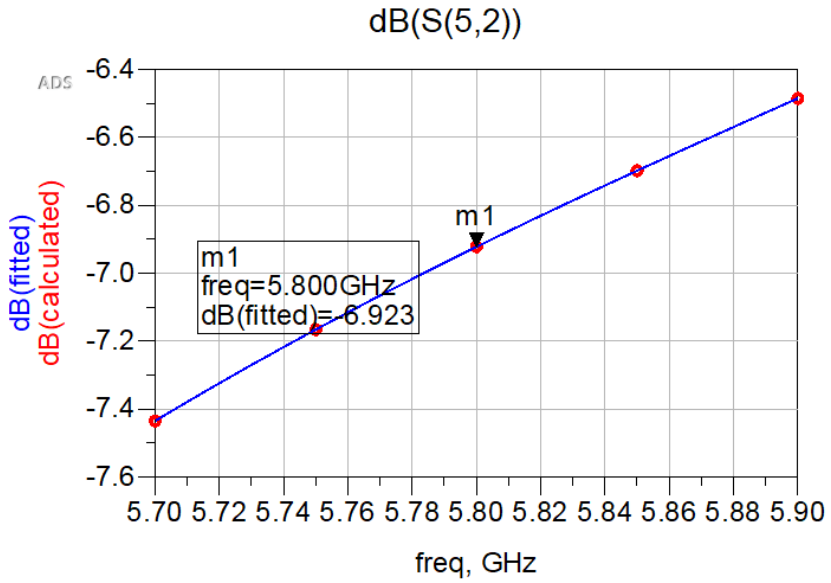


Figure 9.9: S_{52} plot of the Butler matrix.

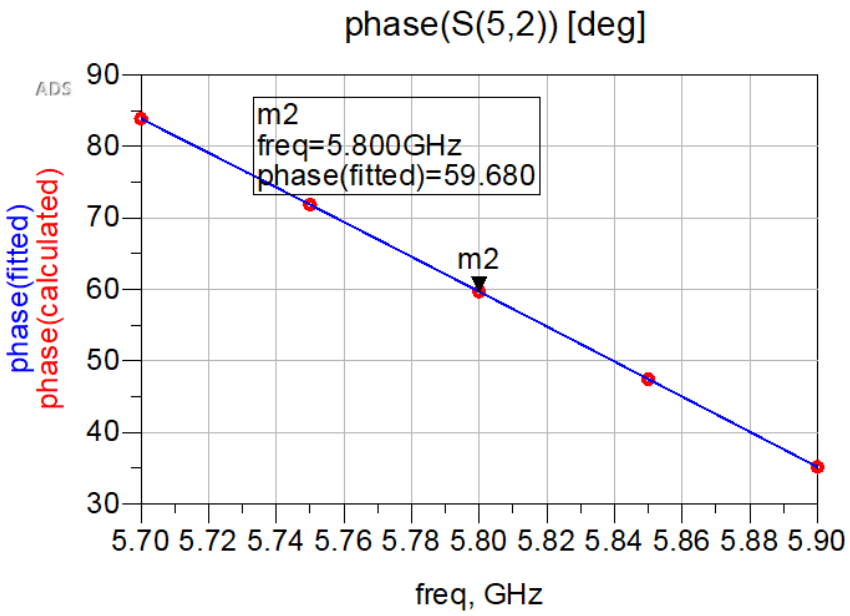


Figure 9.10: S_{52} phase plot of the Butler matrix.

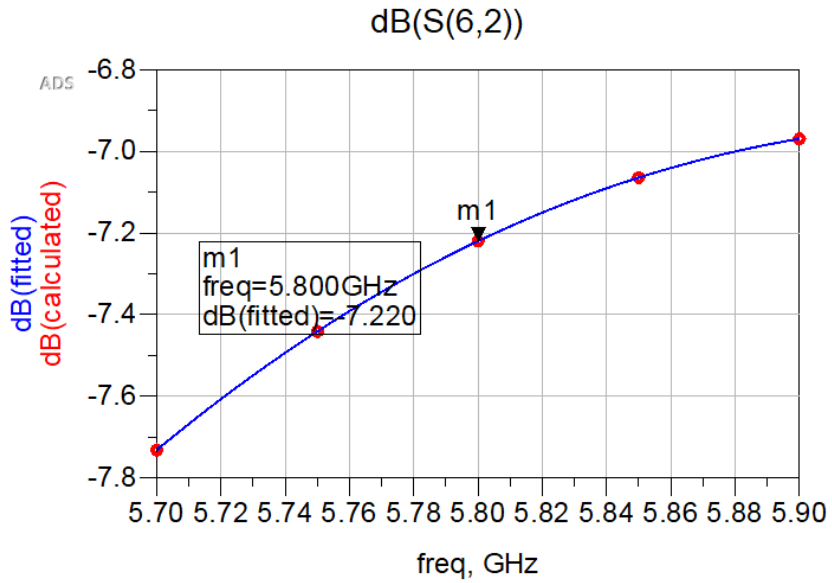


Figure 9.11: S_{62} plot of the Butler matrix.

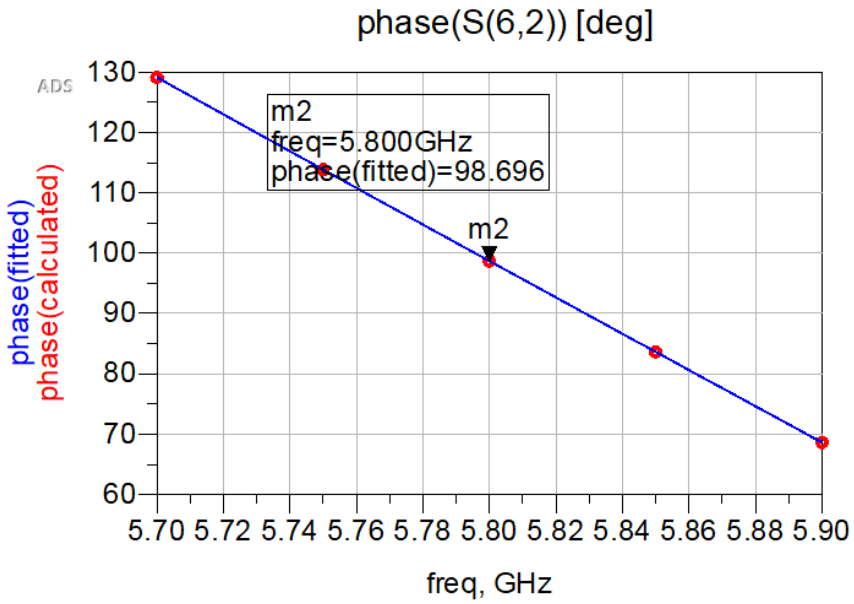


Figure 9.12: S_{62} phase plot of the Butler matrix.

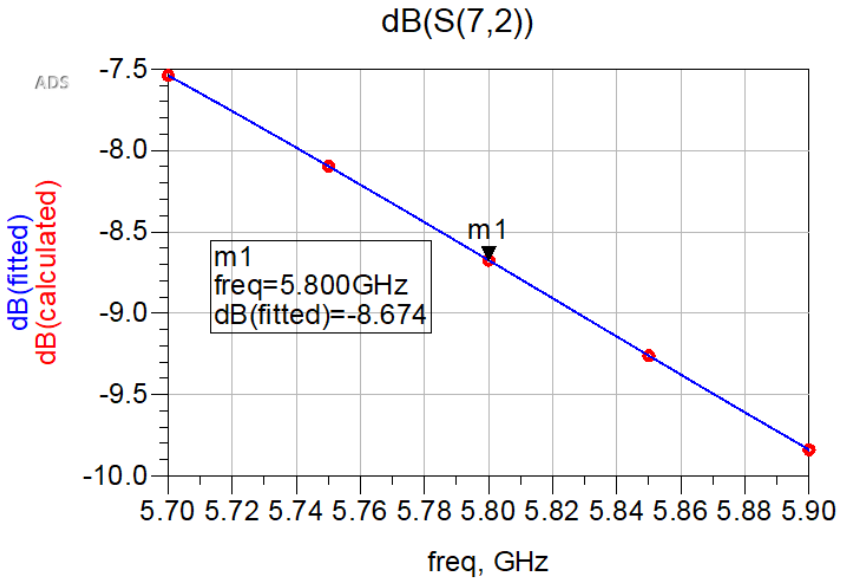


Figure 9.13: S_{72} plot of the Butler matrix.

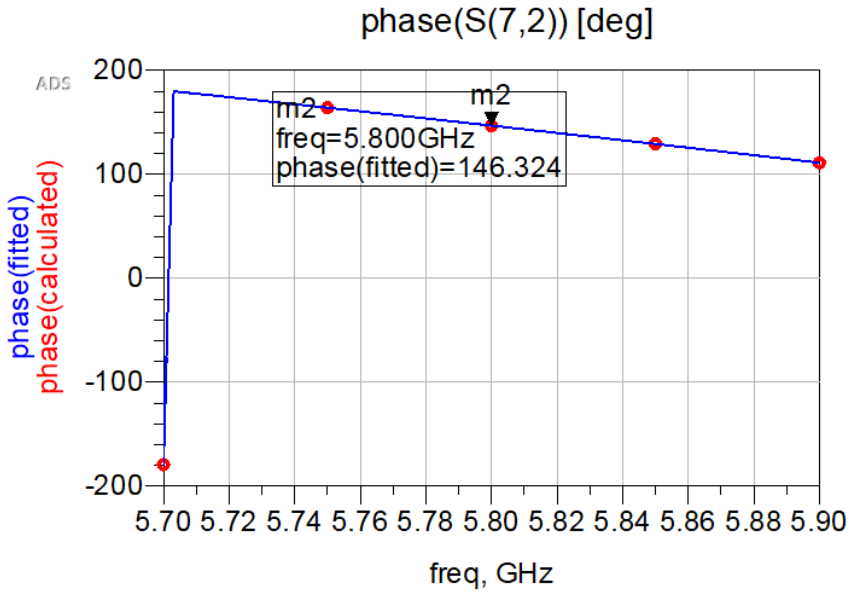


Figure 9.14: S_{72} phase plot of the Butler matrix.

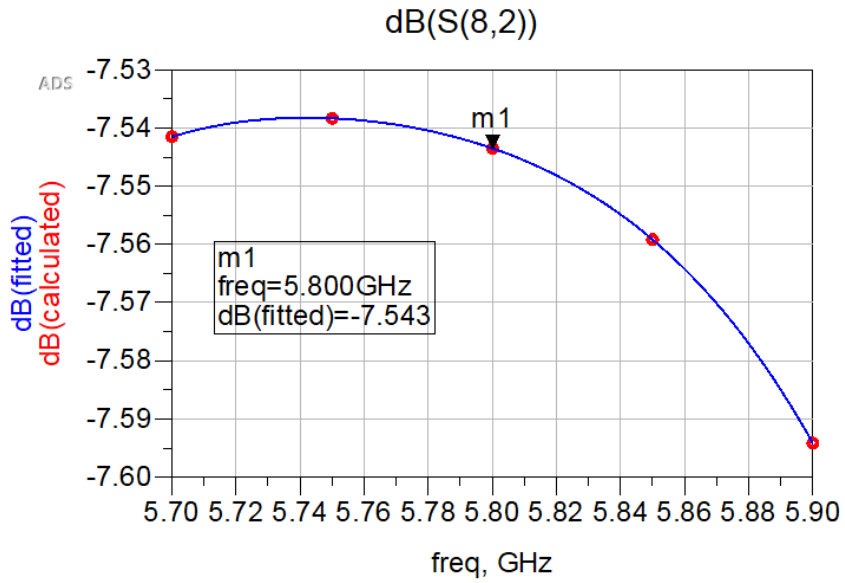


Figure 9.15: S_{82} plot of the Butler matrix.

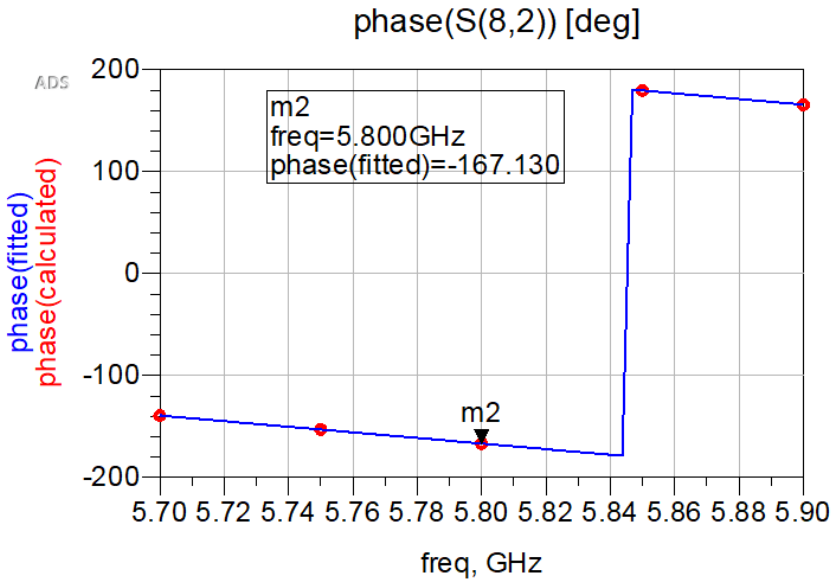


Figure 9.16: S_{82} phase plot of the Butler matrix.

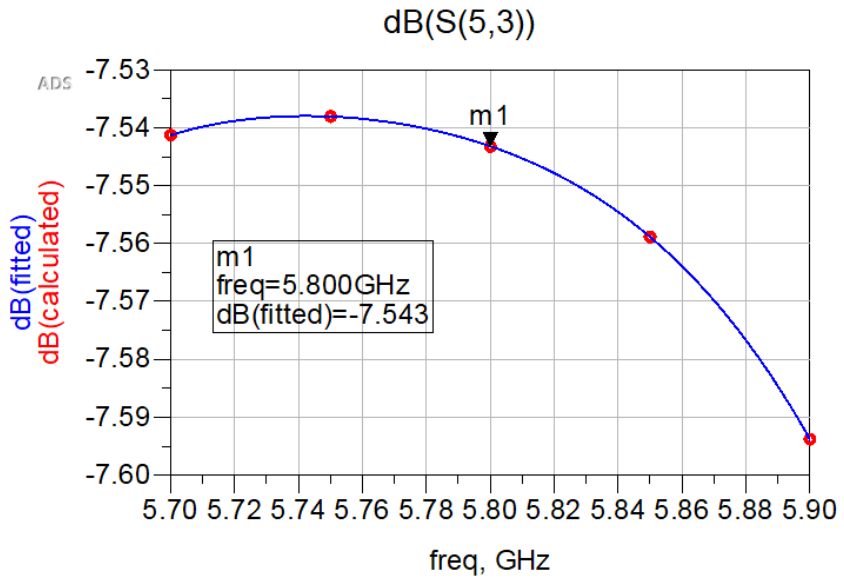


Figure 9.17: S_{53} plot of the Butler matrix.

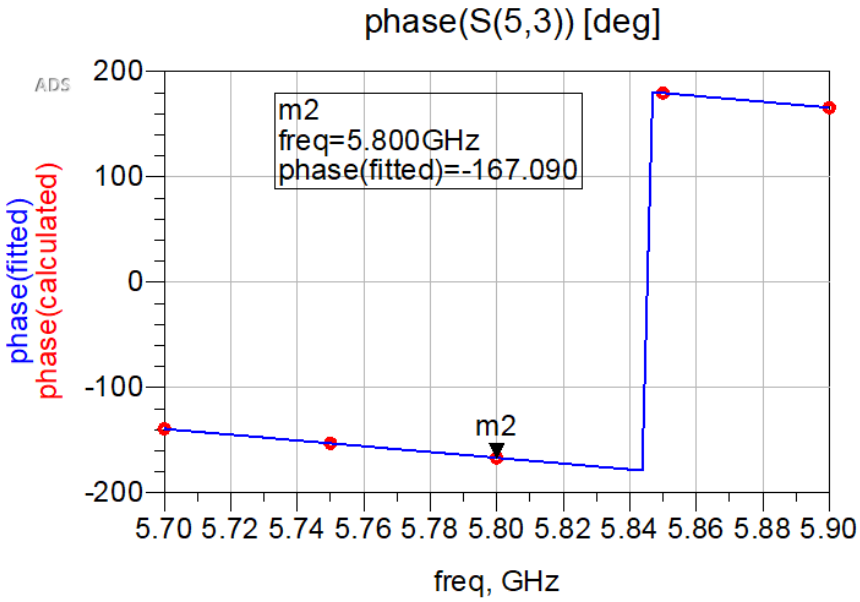


Figure 9.18: S_{53} phase plot of the Butler matrix.

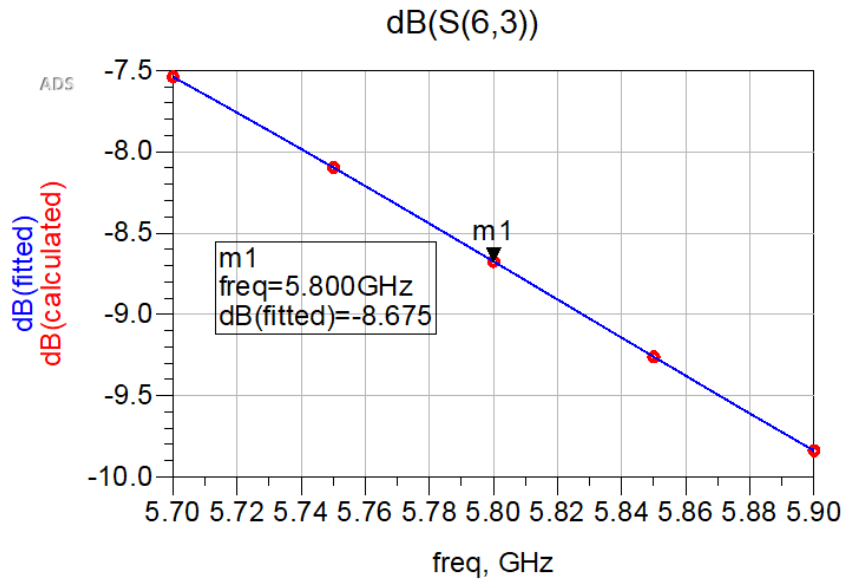


Figure 9.19: S_{63} plot of the Butler matrix.

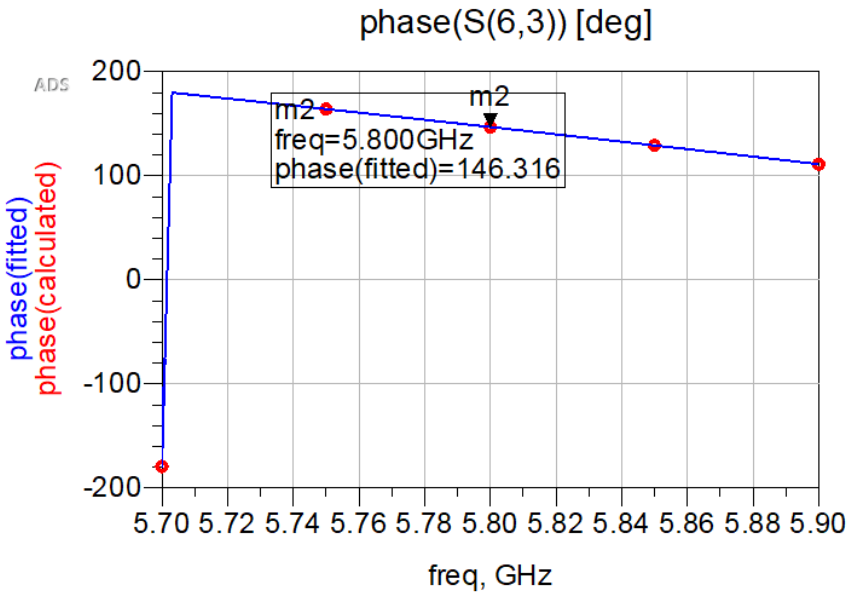


Figure 9.20: S_{63} phase plot of the Butler matrix.

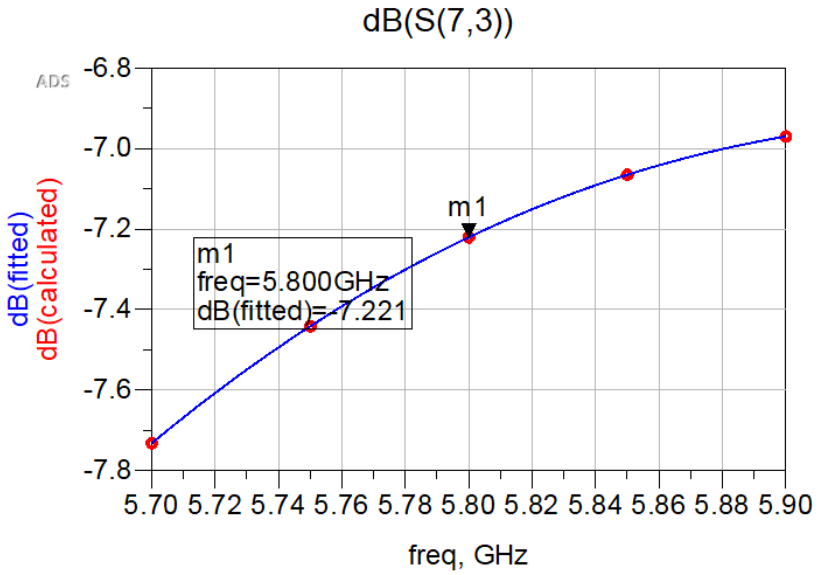


Figure 9.21: S_{73} plot of the Butler matrix.

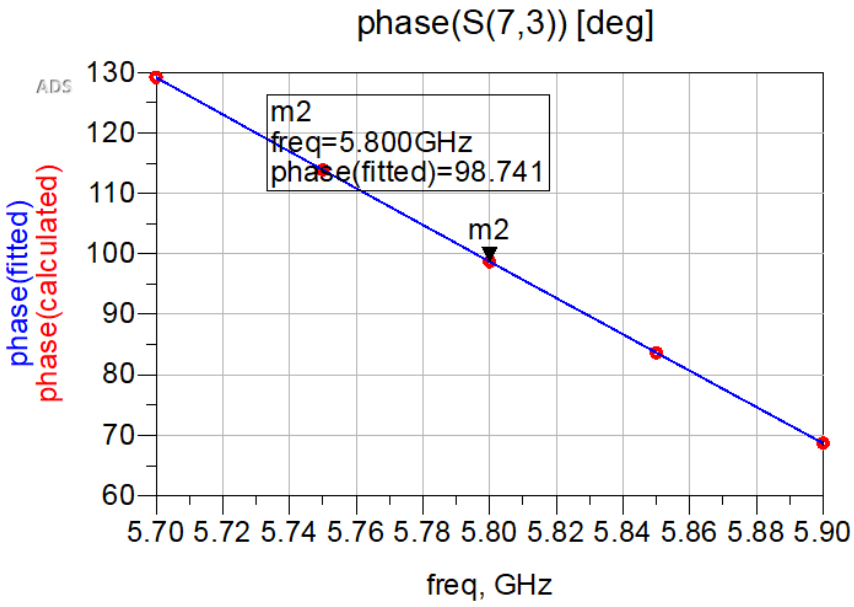


Figure 9.22: S_{73} phase plot of the Butler matrix.

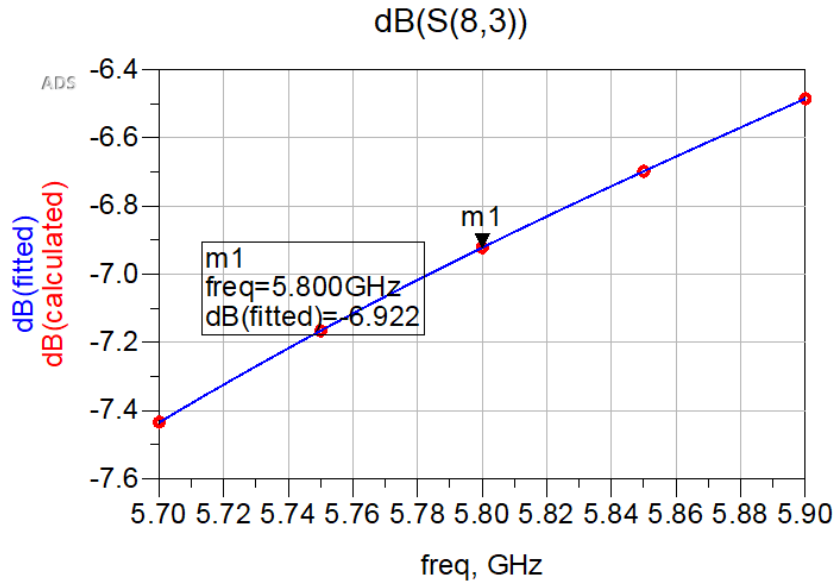


Figure 9.23: S_{83} plot of the Butler matrix.

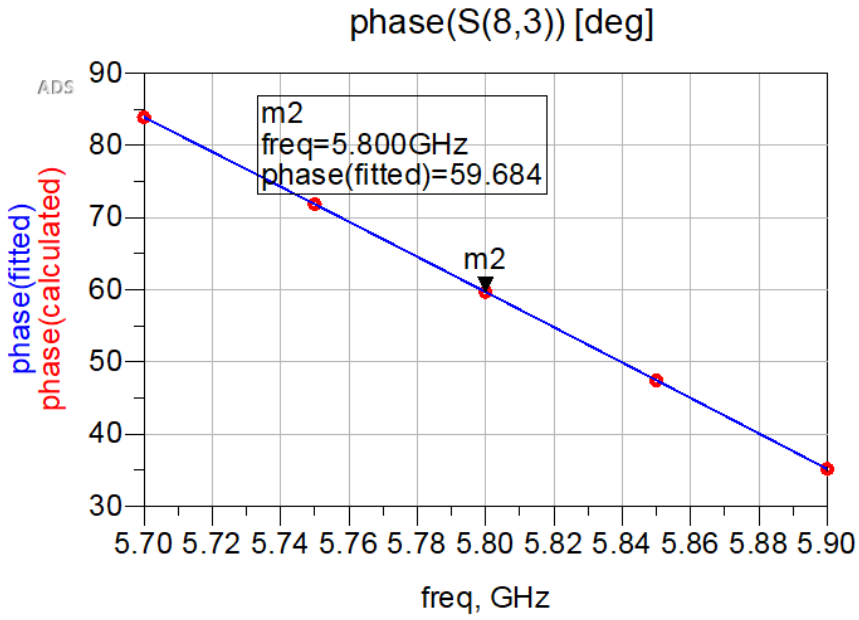


Figure 9.24: S_{83} phase plot of the Butler matrix.

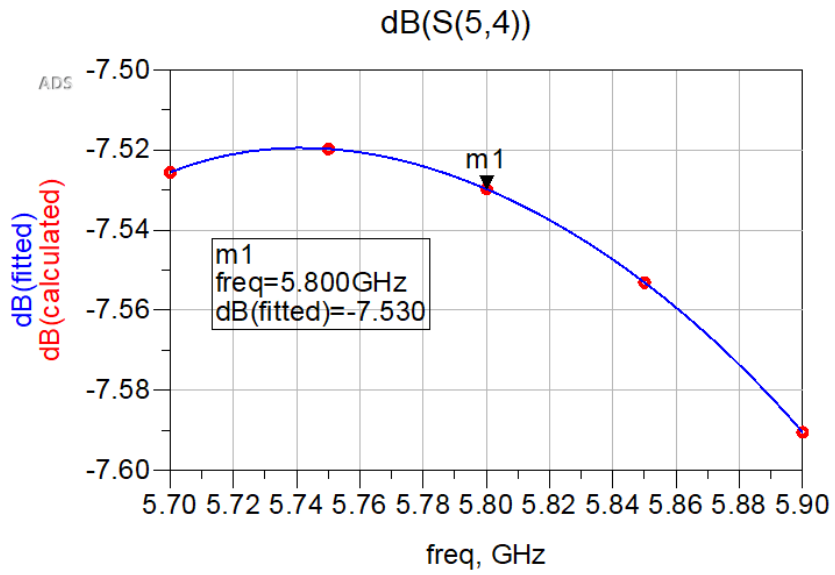


Figure 9.25: S_{54} plot of the Butler matrix.

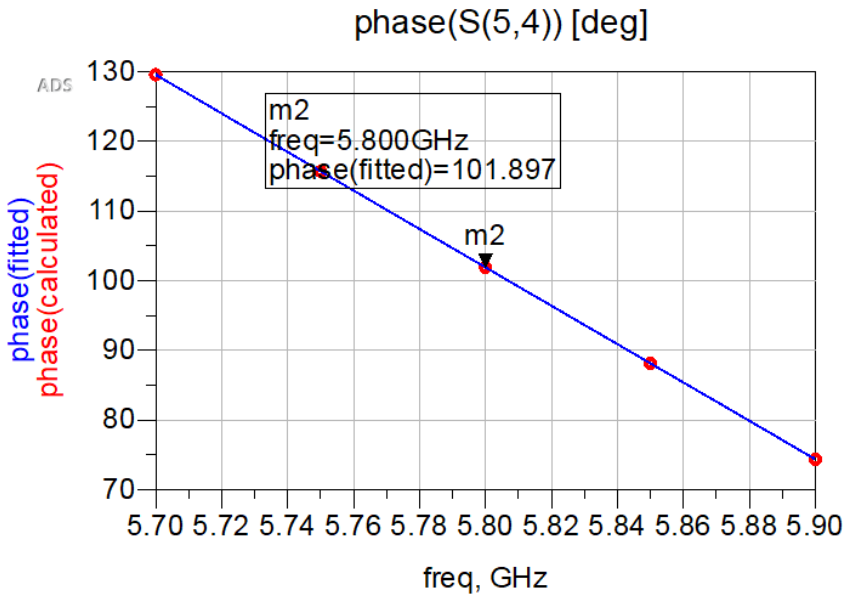


Figure 9.26: S_{54} phase plot of the Butler matrix.

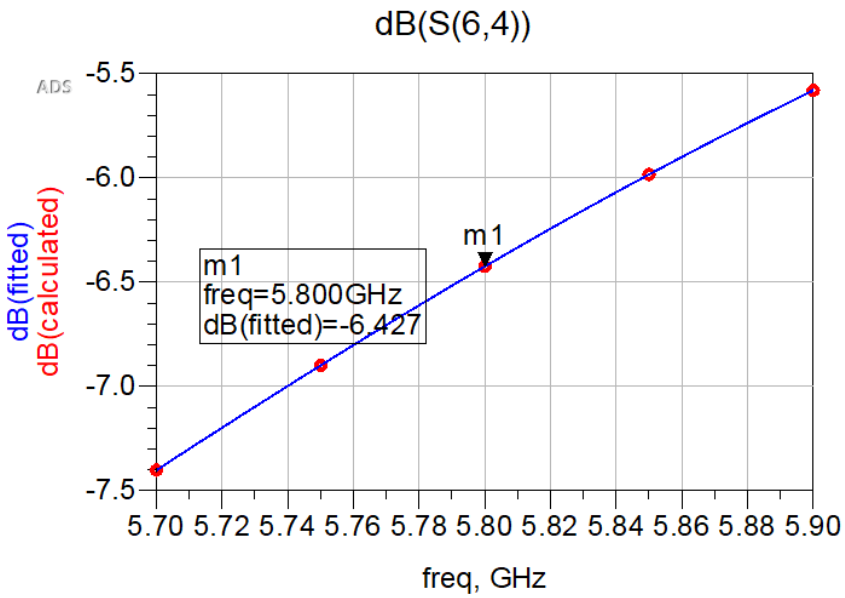


Figure 9.27: S_{64} plot of the Butler matrix.

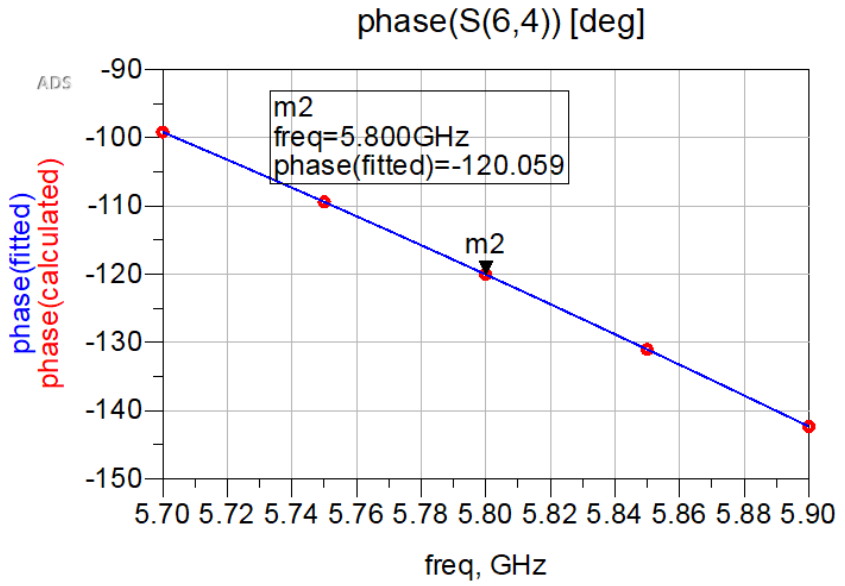


Figure 9.28: S_{64} phase plot of the Butler matrix.

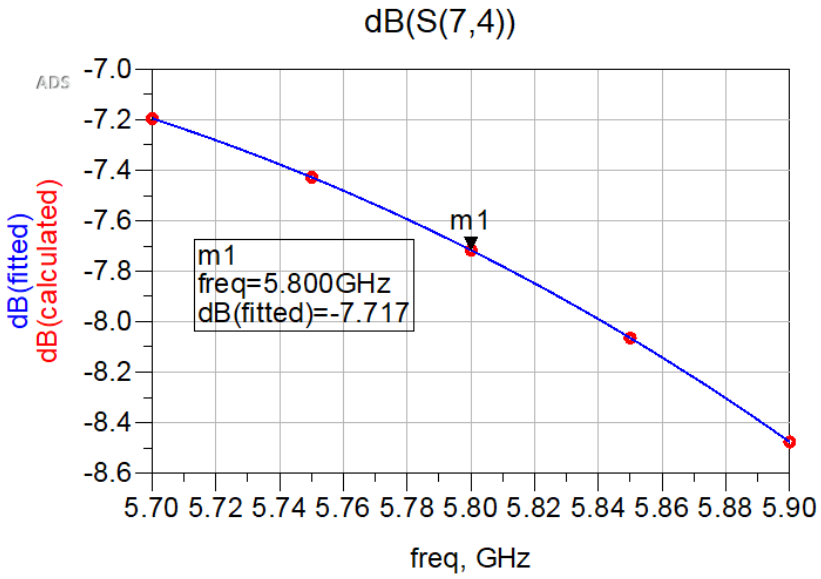


Figure 9.29: S_{74} plot of the Butler matrix.

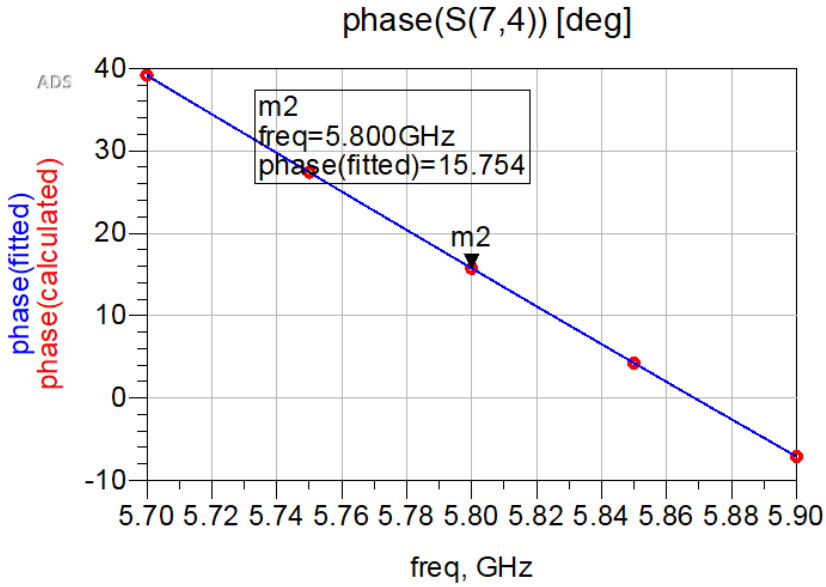


Figure 9.30: S_{74} phase plot of the Butler matrix.

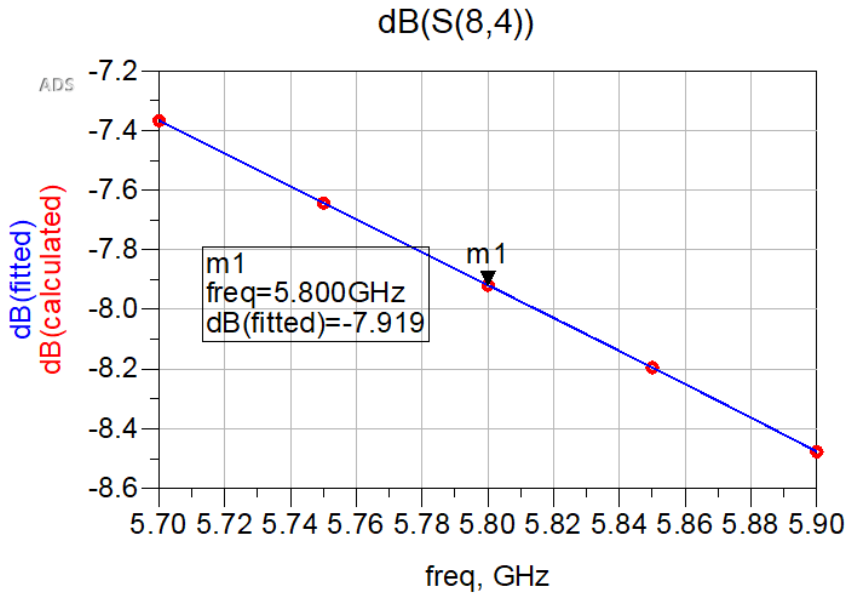


Figure 9.31: S_{84} plot of the Butler matrix.

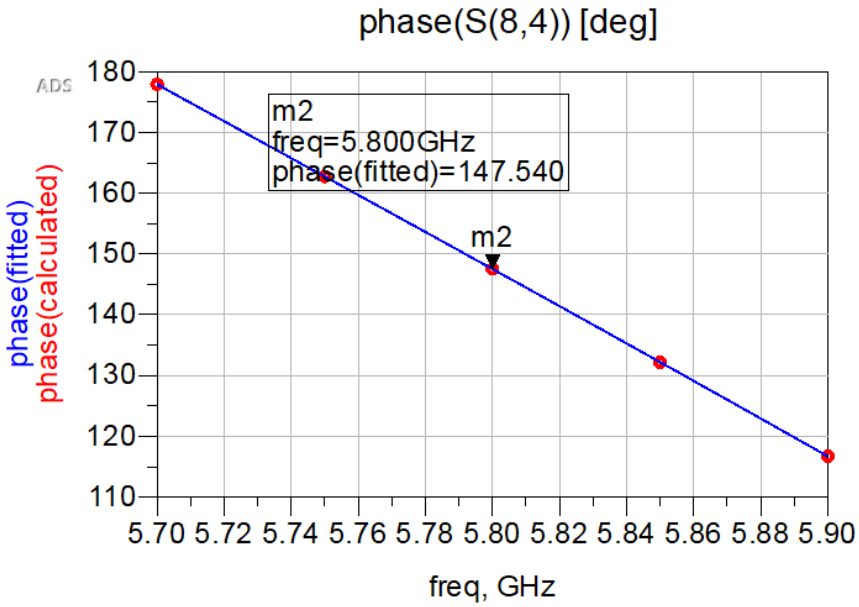


Figure 9.32: S_{84} phase plot of the Butler matrix.

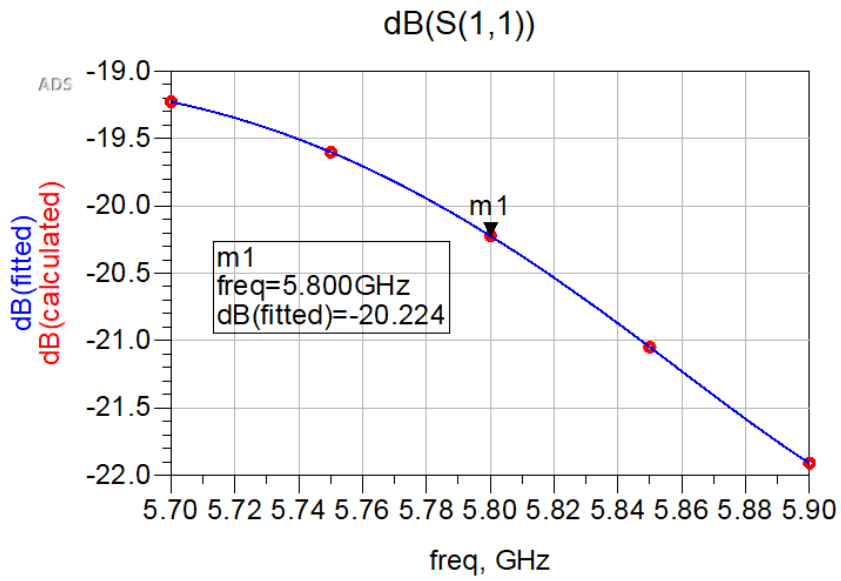


Figure 9.33: S_{11} plot of the Butler matrix.

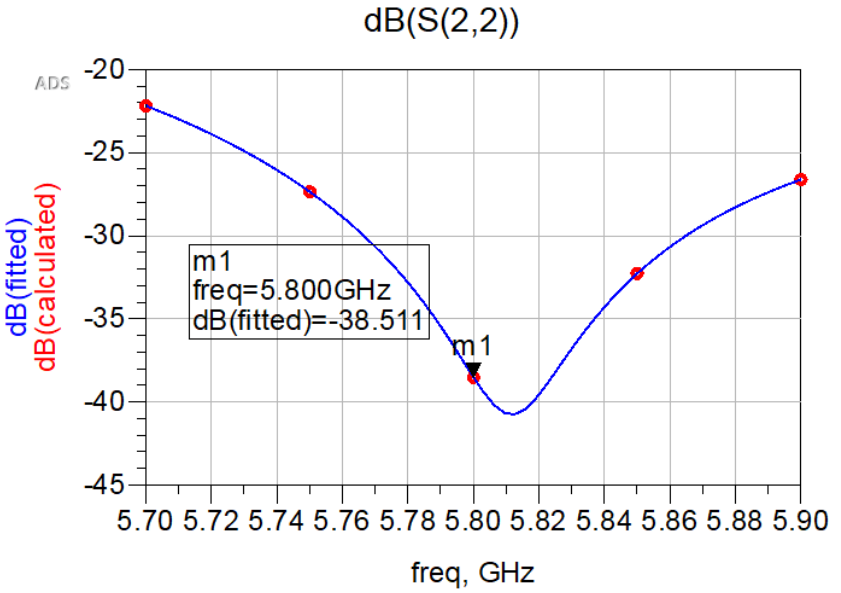


Figure 9.34: S_{22} plot of the Butler matrix.

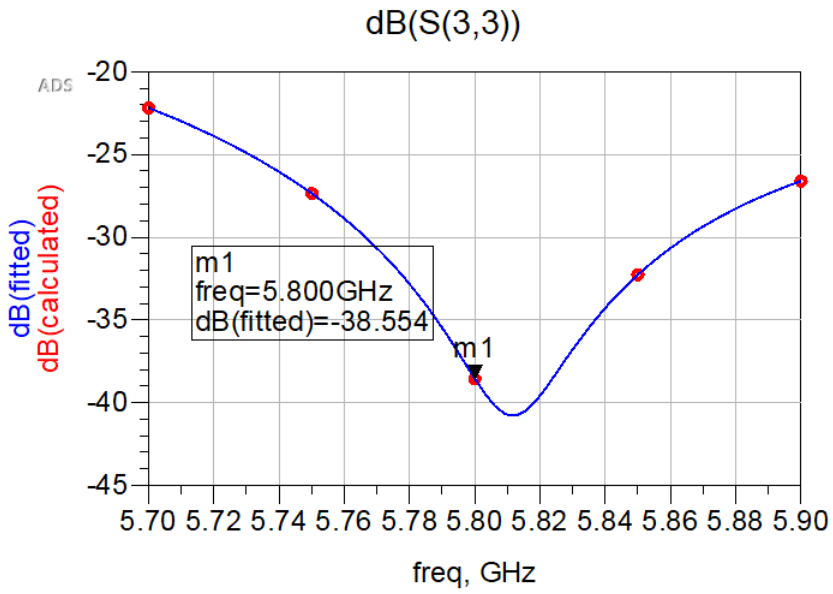


Figure 9.35: S_{33} plot of the Butler matrix.

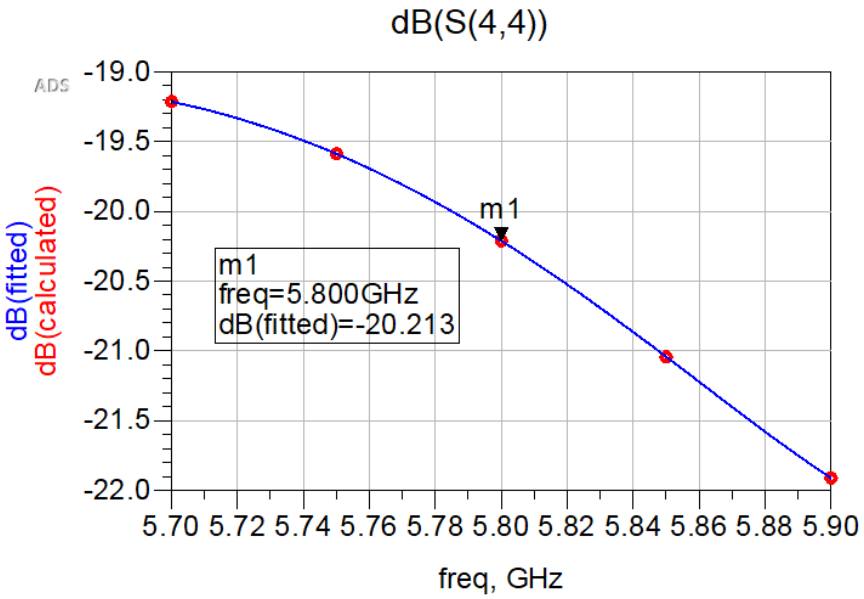


Figure 9.36: S_{44} plot of the Butler matrix.

9.2 Simulated Hub S-parameters

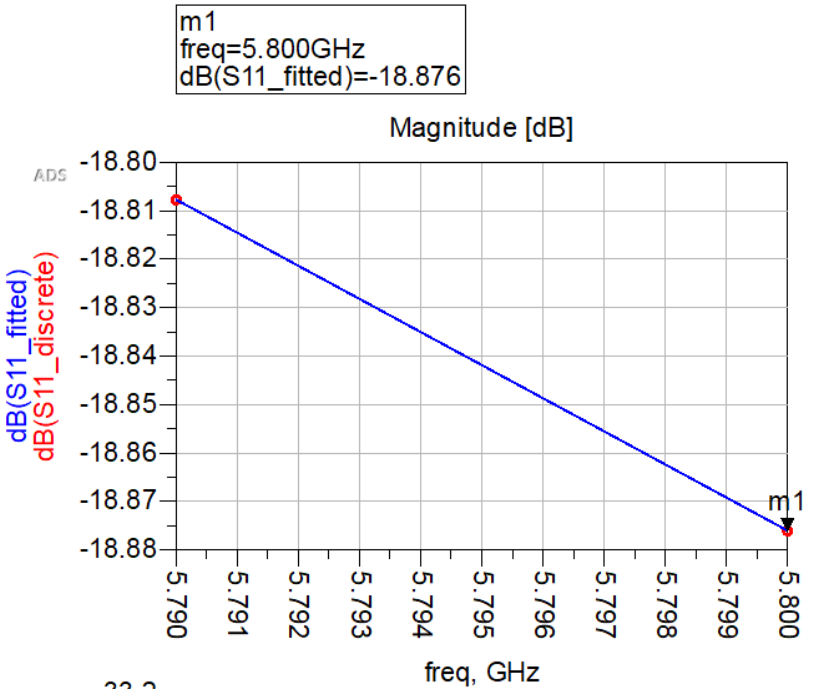


Figure 9.37: S_{11} plot of the hub.

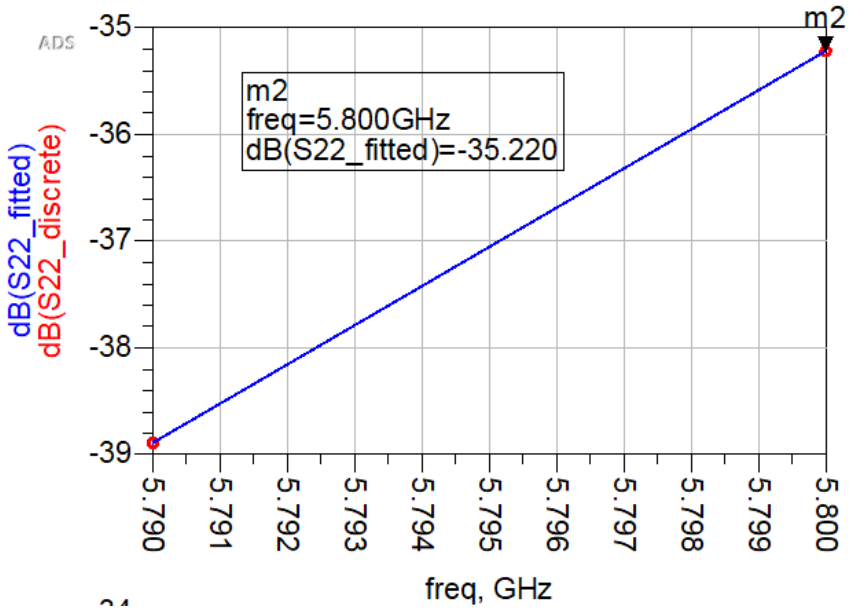


Figure 9.38: S_{22} plot of the hub.

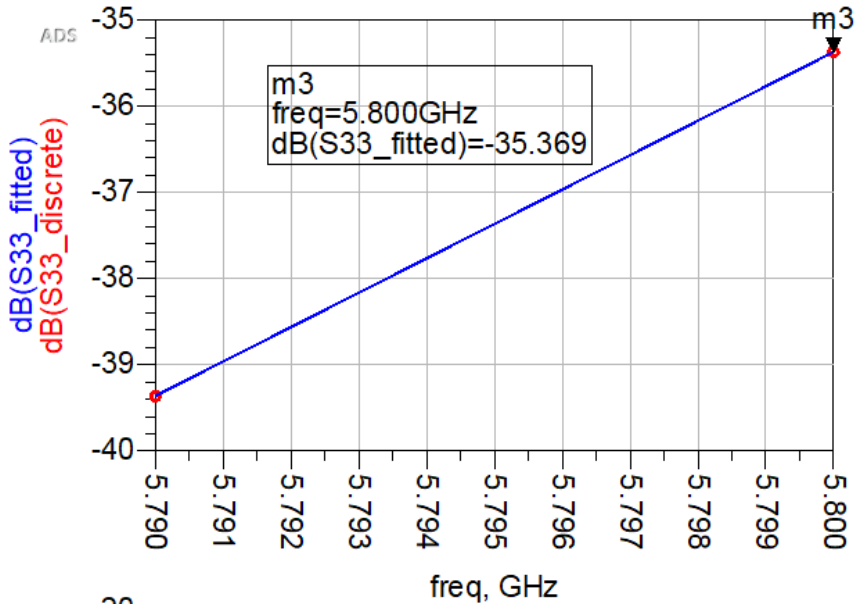


Figure 9.39: S_{33} plot of the hub.

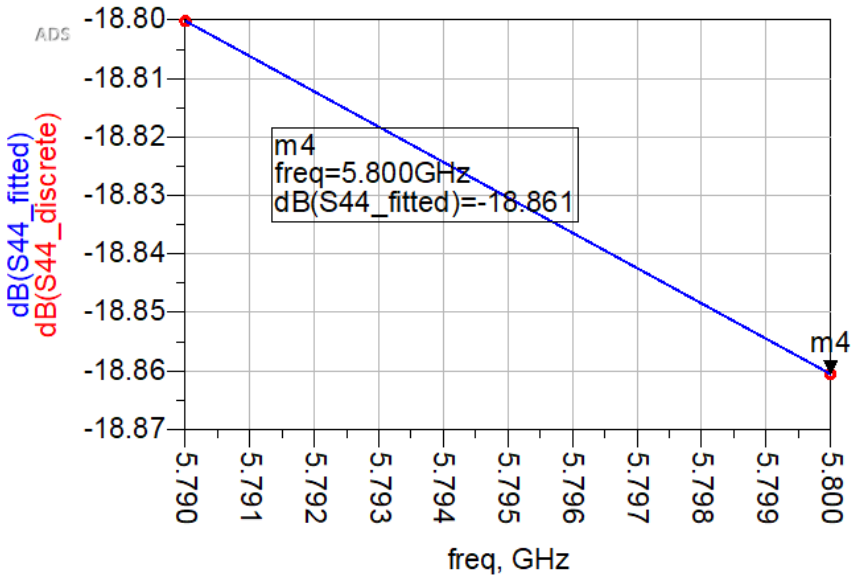


Figure 9.40: S_{44} plot of the hub.

9.3 Measured Hub S-parameters with VNA

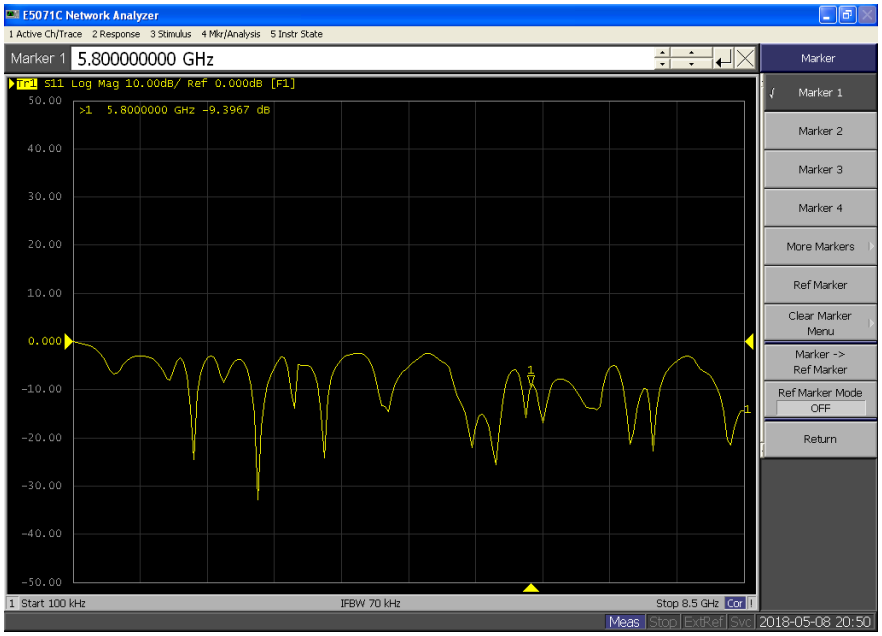


Figure 9.41: S_{11} plot of the hub on VNA.

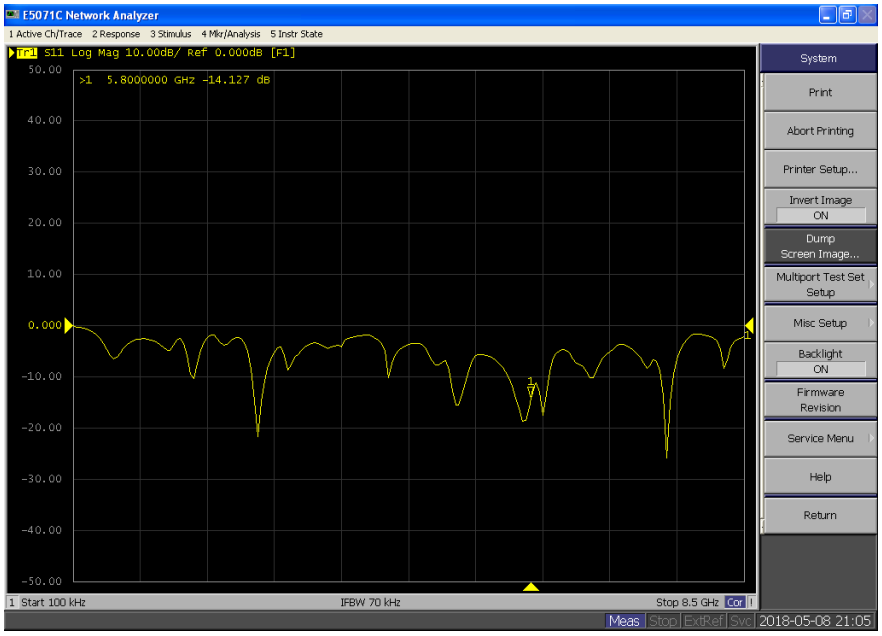


Figure 9.42: S_{22} plot of the hub on VNA.

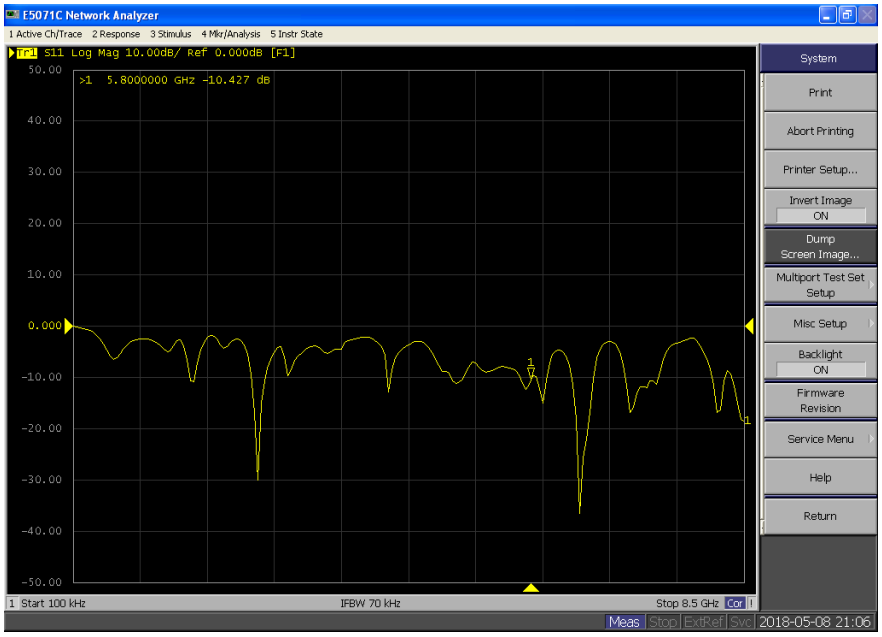


Figure 9.43: S_{33} plot of the hub on VNA.

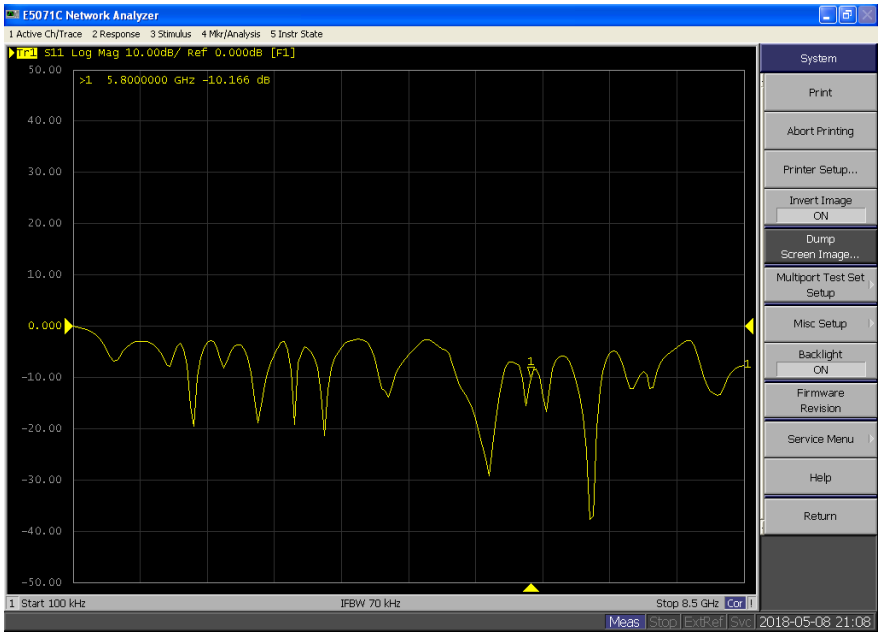


Figure 9.44: S_{44} plot of the hub on VNA.

9.4 RF Circulator S-parameters

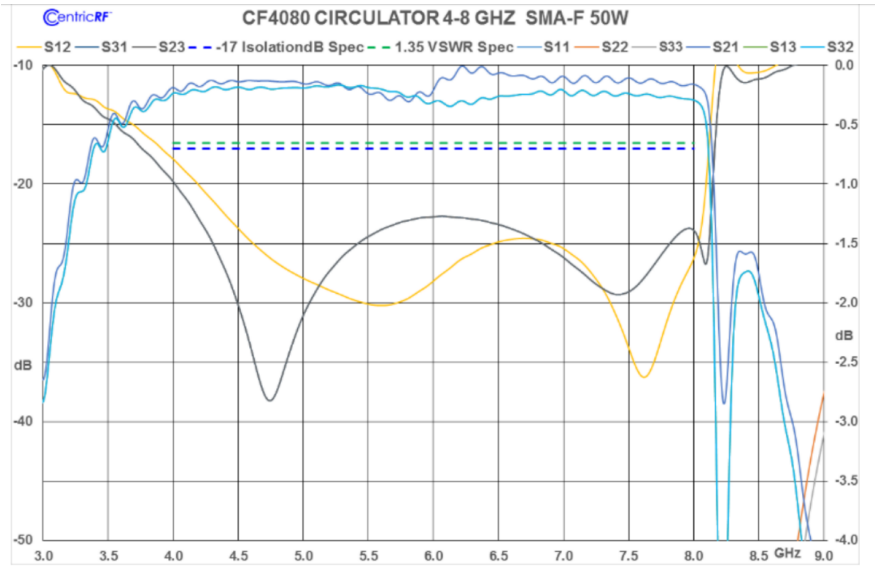


Figure 9.45: Plots of the RF circulator's S-parameters [9].

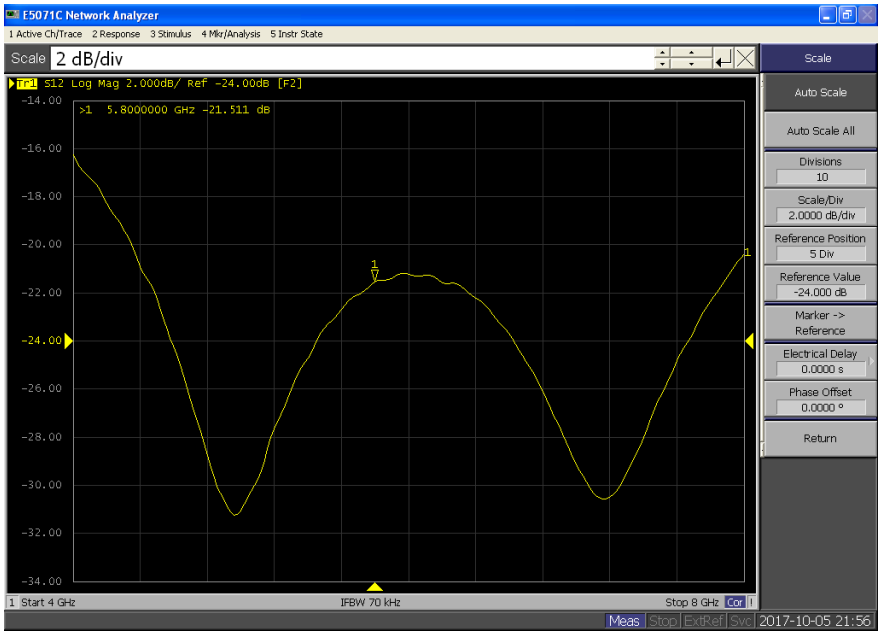


Figure 9.46: S_{12} plot of the circulator on VNA.

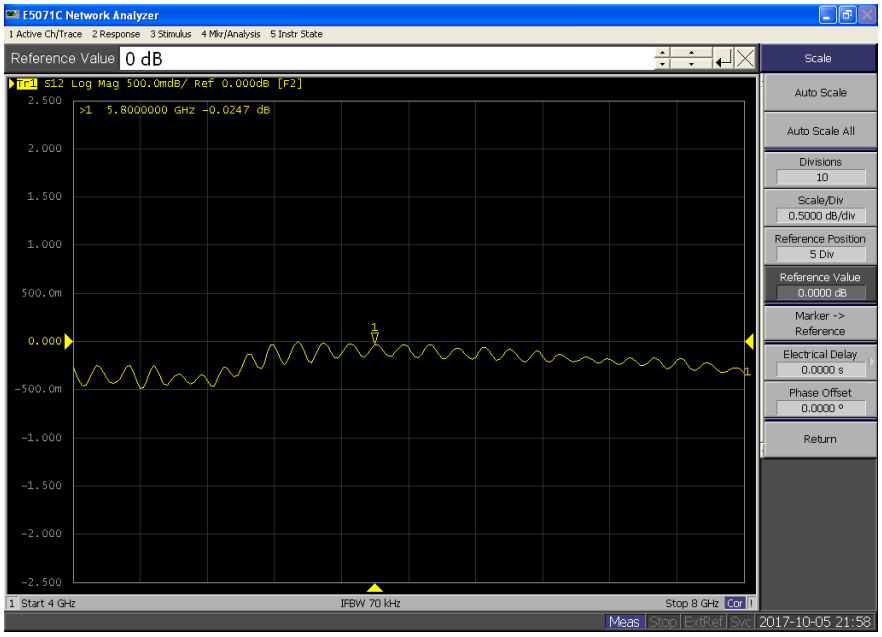


Figure 9.47: S_{13} plot of the circulator on VNA.

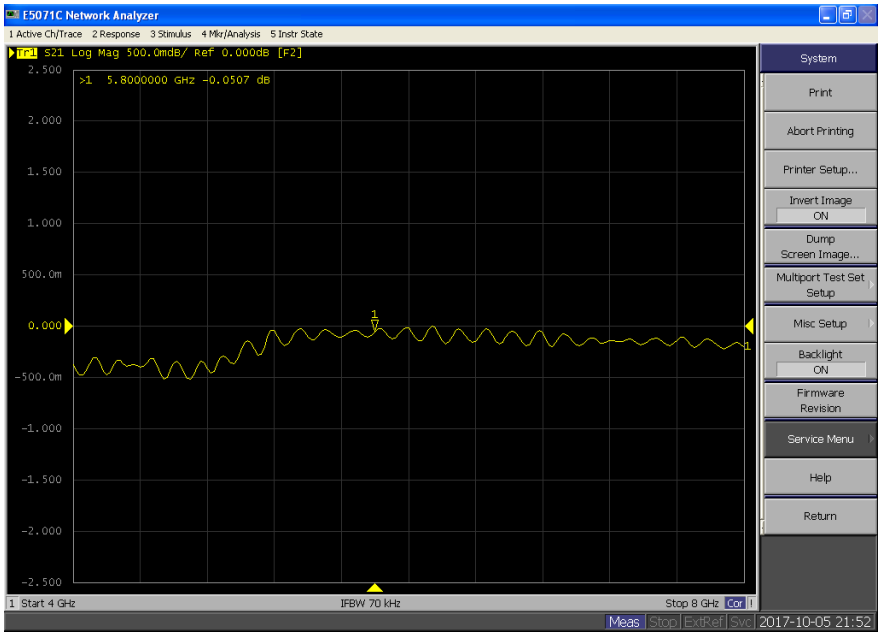


Figure 9.48: S_{21} plot of the circulator on VNA.

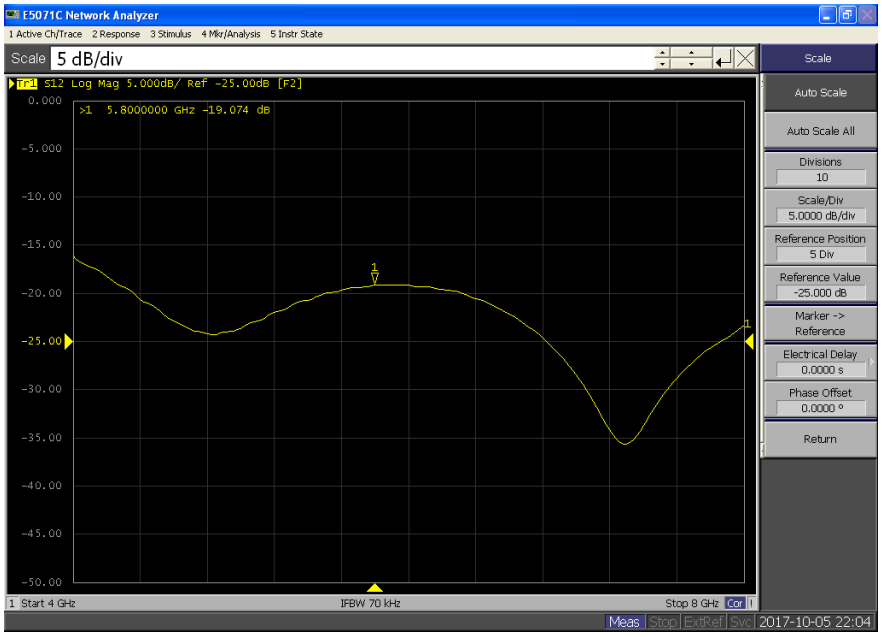


Figure 9.49: S_{23} plot of the circulator on VNA.

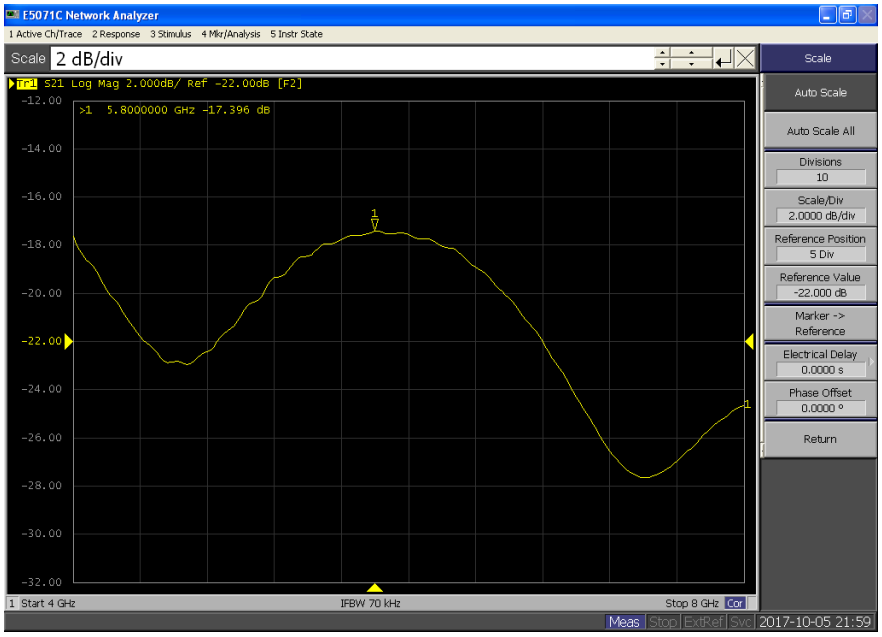


Figure 9.50: S_{31} plot of the circulator on VNA.

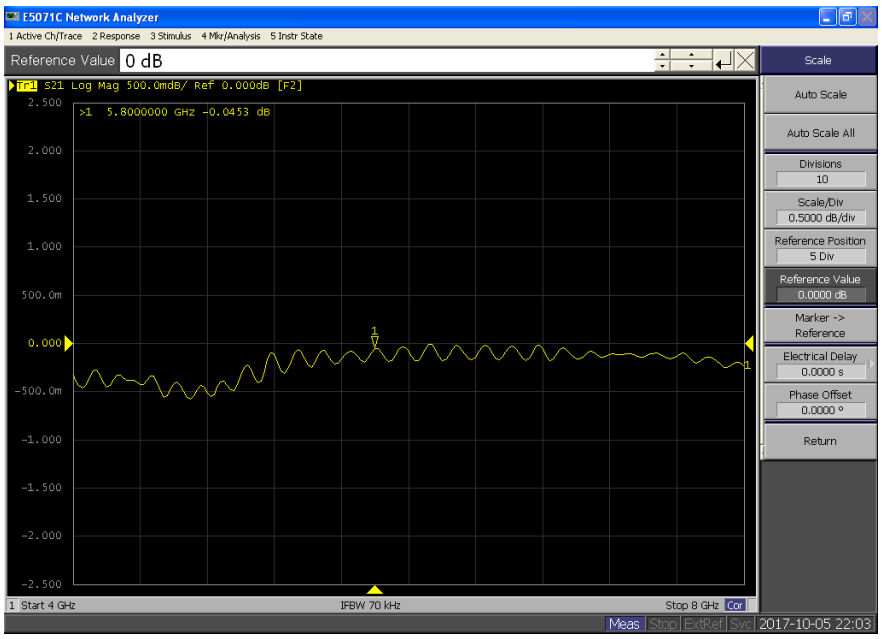


Figure 9.51: S_{32} plot of the circulator on VNA.

9.5 RF to DC Converter Datasheet

ANALOG DEVICES

1 MHz to 8 GHz, 70 dB Logarithmic Detector/Controller

Data Sheet **AD8318**

FEATURES

Wide bandwidth: 1 MHz to 8 GHz
High accuracy: ±1.0 dB over 55 dB range (f < 5.8 GHz)
Stability over temperature: ±0.5 dB
Low noise measurement/controller output (VOUT)
Pulse response time: 10 ns/12 ns (fall/rise)
Integrated temperature sensor
Small footprint LFCSP
Power-down feature: <1.5 mW at 5 V
Single-supply operation: 5 V at 68 mA
Fabricated using high speed SiGe process

APPLICATIONS

RF transmitter PA setpoint control and level monitoring
RSSI measurement in base stations, WLAN, WiMAX, and radars

FUNCTIONAL BLOCK DIAGRAM

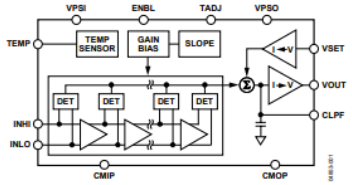


Figure 1.

GENERAL DESCRIPTION

The AD8318 is a demodulating logarithmic amplifier, capable of accurately converting an RF input signal to a corresponding decibel-scaled output voltage. It employs the progressive compression technique over a cascaded amplifier chain, each stage of which is equipped with a detector cell. The device is used in measurement or controller mode. The AD8318 maintains accurate log conformance for signals of 1 MHz to 6 GHz and provides useful operation to 8 GHz. The input range is typically 60 dB (referenced to 50 Ω) with error less than ±1 dB. The AD8318 has a 10 ns response time that enables RF burst detection to beyond 45 MHz. The device provides unprecedented logarithmic intercept stability vs. ambient temperature conditions. A 2 mV/°C slope temperature sensor output is also provided for additional system monitoring. A single supply of 5 V is required. Current consumption is typically 68 mA. Power consumption decreases to <1.5 mW when the device is disabled.

The AD8318 can be configured to provide a control voltage to a VGA, such as a power amplifier or a measurement output, from Pin VOUT. Because the output can be used for controller applications, wideband noise is minimal.

In this mode, the setpoint control voltage is applied to VSET. The feedback loop through an RF amplifier is closed via VOUT, the output of which regulates the amplifier output to a magnitude corresponding to VSET. The AD8318 provides 0 V to 4.9 V output capability at the VOUT pin, suitable for controller applications. As a measurement device, Pin VOUT is externally connected to VSET to produce an output voltage, V_{OUT}, which is a decreasing linear-in-dB function of the RF input signal amplitude.

The logarithmic slope is nominally −25 mV/dB but can be adjusted by scaling the feedback voltage from VOUT to the VSET interface. The intercept is 20 dBm (referenced to 50 Ω, CW input) using the INHI input. These parameters are very stable against supply and temperature variations.

The AD8318 is fabricated on a SiGe bipolar IC process and is available in a 4 mm × 4 mm, 16-lead LFCSP for the operating temperature range of −40°C to +85°C.

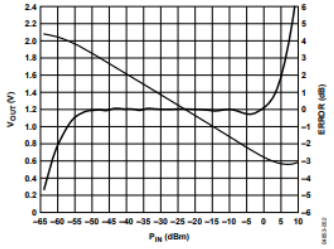


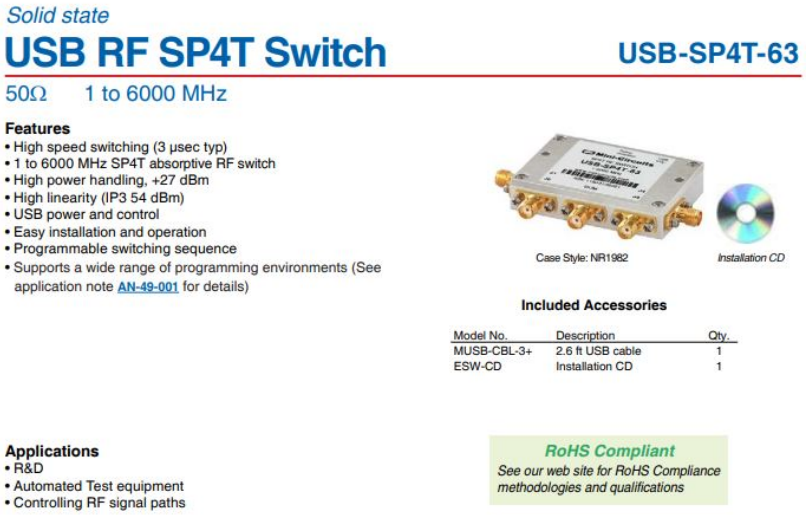
Figure 2. Typical Logarithmic Response and Error vs. Input Amplitude at 5.8 GHz

Figure 9.52: Cover page of the datasheet for the RF to DC Converter.

f = 5.8 GHz	R_{TADJ} = 1000 Ω		
Input Impedance		33||0.59	Ω||pF
±3 dB Dynamic Range	T_A = 25°C	70	dB
±1 dB Dynamic Range	T_A = 25°C	57	dB
	−40°C < T_A < +85°C	48	dB
Maximum Input Level	±1 dB error	−1	dBm
Minimum Input Level	±1 dB error	−58	dBm
Slope		−24.3	mV/dB
Intercept		25	dBm
Output Voltage—High Power In	P_{IN} = −10 dBm	0.86	V
Output Voltage—Low Power In	P_{IN} = −40 dBm	1.59	V
Temperature Sensitivity	P_{IN} = −10 dBm		
	25°C ≤ T_A ≤ 85°C	0.0033	dB/°C
	−40°C ≤ T_A ≤ +25°C	0.0069	dB/°C

Figure 9.53: Specifications of the RF to DC Converter, which includes RF power (input) and DC voltage (output).

9.6 RF Circulator Datasheet



Solid state

USB RF SP4T Switch **USB-SP4T-63**

50Ω 1 to 6000 MHz

Features

- High speed switching (3 µsec typ)
- 1 to 6000 MHz SP4T absorptive RF switch
- High power handling, +27 dBm
- High linearity (IP3 54 dBm)
- USB power and control
- Easy installation and operation
- Programmable switching sequence
- Supports a wide range of programming environments (See application note AN-49-001 for details)

Case Style: NR1982 *Installation CD*

Included Accessories

Model No.	Description	Qty.
MUSB-CBL-3+	2.6 ft USB cable	1
ESW-CD	Installation CD	1

Applications

- R&D
- Automated Test equipment
- Controlling RF signal paths

RoHS Compliant

See our web site for RoHS Compliance methodologies and qualifications

Mini-Circuits RF Switch Control Program for USB Solid State RF Switch

Figure 9.54: Cover page of the datasheet for the RF switch.

USB RF SP4T Switch — USB-SP4T-63

Electrical Specifications

Parameter	Port	Conditions	Min.	Typ.	Max.	Units
Operating Frequency			1		6000	MHz
Insertion Loss	COM to any active port	1 to 3000 MHz	–	1.0	2.0	dB
		3000 to 6000 MHz	–	1.6	3.0	
Isolation	Between ports J1,J2,J3, and J4	1 to 500 MHz	50	85	–	dB
		500 to 5000 MHz	35	60		
		5000 to 6000 MHz	33	55	–	
	COM to any terminated port	1 to 500 MHz	55	85		
		500 to 5000 MHz	30	50		
		5000 to 6000 MHz	25	40	–	
VSWR	COM port	1 to 3000 MHz	–	1.10	1.40	:1
		3000 to 6000 MHz	–	1.15	1.60	
	Any port connected to COM	1 to 3000 MHz	–	1.20	1.50	
		3000 to 6000 MHz	–	1.20	1.55	
	Any terminated port	1 to 3000 MHz	–	1.10	1.60	
		3000 to 6000 MHz	–	1.25	2.00	
Power Input @1 dB Compression [1,2]	COM to any active port	10 to 6000 MHz	30	–	–	dBm
IP3 [3]	COM to any active port	10 to 6000 MHz	–	54	–	dBm
Switching Time	–	Note 4	–	3	–	µsec
Minimum dwell time	–	Using switching sequence function	–	5	–	µsec
Rated voltage	USB port	–	4.75	5	5.25	V
Rated Current		–	–	30	80	mA
Operating RF Input Power	COM to any active port	Hot Switching	–	–	+17	dBm
	Any terminated port	–	–	–	+17	
	COM to any active port	Through path [1]	–	–	+27	

[1] Max operating power degrades linearly below 10 MHz to +22 dBm at 1 MHz.
[2] Note absolute maximum ratings in table below
[3] Tested with 1 MHz span between signals.
[4] Specified without communication delays. Switching time spec represents the time that the RF signal paths are interrupted during switching.

Minimum System Requirements

Interface	USB HID
Host operating system - USB Control	**Windows 32/64 Bit operating system:** Windows 98®, Windows XP®, Windows Vista®, Windows 7®, Windows 8® **Linux® support:** 32/64 Bit operating system
Hardware	Pentium® II or better

Connections

RF Switch (J1, J2, J3, J4, COM)	(SMA female)
USB	(USB type Mini-B receptacle)

Absolute Maximum Ratings

Operating Temperature	0°C to 50°C
Storage Temperature	-20°C to 60°C
DC supply voltage max.	6V
RF power @ 1 -6000 MHz into termination	+20 dBm
RF power @ 10 -6000 MHz into COM or active port	+30 dBm
RF power @ 1 -10 MHz into COM or active port	+25 dBm
DC voltage @ RF Ports	16V

Permanent damage may occur if any of these limits are exceeded. Operating in the range between operating power limits and absolute maximum ratings for extended periods of time may result in reduced life and reliability.

Figure 9.55: Specifications of the RF switch.

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