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Process Optimization for Carbon Nanotubes-On-Graphene Fabrication

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PROCESS OPTIMIZATION FOR CARBON NANOTUBES-ON-GRAPHENE FABRICATION

By

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SENIOR DESIGN PROJECT REPORT

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Abstract

Because of their superior thermal and electrical properties, carbon nanotubes (CNTs) and graphene (Gr) are promising candidates to replace copper and tungsten as interconnect materials in the most advanced integrated circuit technologies. We explore a three-dimensional all-carbon interconnect structure, consisting of vertically aligned CNTs grown directly on multi-layer graphene (MLG). The objective is to grow the CNTs with little or no damage to the graphene underlayer. We start with fabricating test structures using both plasma enhanced chemical vapor deposition (PECVD) and thermal CVD throughout the CNT growth process to confirm the results of previous work of our research group. We then proceed to design a process to grow CNTs using PECVD in order to achieve a test structure with not only vertically aligned CNTs, but also a conductive graphene underlayer. In order to achieve this, we vary the plasma conditions within the reactor during the CNT growth process and analyze the fabricated test structure using a scanning electron microscope (SEM) and a wafer probe station. Through our analysis we are able to determine the viability of our designed process. We are able to produce a test structure with partially aligned CNTs and an intact graphene underlayer by lowering the DC voltage of the plasma used in the PECVD process. As a result, we find that resistance of the sample is comparable to that of plain graphene. Three-dimensional all-carbon nanostructures such as the ones fabricated in our project can lead to functionalization of such structures as building blocks for future on-chip interconnects.

Acknowledgements

We acknowledge the strong support and guidance of our project advisor, Dr. Cary Yang, along with our research team members, Richard Senegor and Dayou Luo. We express our appreciation for the Santa Clara University School of Engineering faculty and staff for their support in the form of encouragements, guidance, and access to their state-of-the-art Center for Nanostructures laboratories on campus and in NASA Ames Research Center that made our research possible.

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Chapter 1: Introduction

1.1 Interconnect Challenges

Integrated circuits (IC) or chips are the brains and drivers of all electronic systems. Each IC consists of a large number of components such as transistors, diodes, capacitors, and resistors, as well as the wires connecting these components, known as interconnects. These interconnects, usually made out of copper (Cu) and tungsten (W) in the current IC technology, facilitate signal transmission throughout the entire chip. A typical electronic system fabricated on a printed circuit board consists of several ICs such as that shown in Figure 1. Because ICs are essential for the electronics industry, integrated circuits must utilize technology that is not only high-performing but is also as reliable as possible. In 1965 Gordon Moore predicted that the number of transistors in ICs would double every year [1], which he revised in 1975 to doubling every two years [2]. This prediction, more commonly known as "Moore's Law", is not science-based, but merely a projection that has nonetheless shaped the IC industry. This trend has allowed electronics to be scaled up in power but also scaled down in component feature size. Currently, the IC industry has been able to keep up with the increasing number of on-chip components while simultaneously decreasing the size of each component, and to a lesser extent, decreasing the linewidths of the interconnects. As the minimum feature size (traditionally the transistor channel length until the 28 nm-technology node) scales down to sub-30 nm, the chip performance is limited by its ability to dissipate the Joule heat generated during its operation [3]. Much of such generated heat is due to high current densities through the interconnects. Such reduced linewidths and high current densities pose additional chip performance and reliability challenges as described below.

Figure 2 shows the cross-section of an IC consisting of multiple metal layers connected by Cu interconnect vias. The transistors are connected to the first metal layer using W plugs. As the interconnect linewidth decreases, both the metal resistivity and current density increase, giving rise to degradation in performance and reliability, respectively. As the interconnect linewidths scale down to the nanoscale, they become comparable to the electron mean free path; resulting in increased scatterings from the interconnect wire interior walls, known as surface scattering. At the same time, the reduced linewidth decreases the average size of polycrystalline Cu grains, which in turn, increases scatterings from the grain boundaries. Thus, the Cu resistivity increases significantly with decreasing linewidth in the nanoscale, as shown in Figure 3.

Further, the reduction of the interconnect linewidth results in an increase in current density approaching or exceeding the metal current-carrying capacity, giving rise to electromigration in the metal [4]. Chip failure can occur when the maximum current density in the chip, J_{max}, exceeds the current-carrying capacity of Cu (about 2 MA/cm^2 for bulk Cu), as illustrated in Figure 4. Current-carrying capacity typically decreases with decreasing linewidth, thus becoming a major reliability problem for sub-30 nm technology chips [5]. Similar performance and reliability challenges exist for W [6] and continued downward scaling in feature size is expected to exacerbate these challenges.

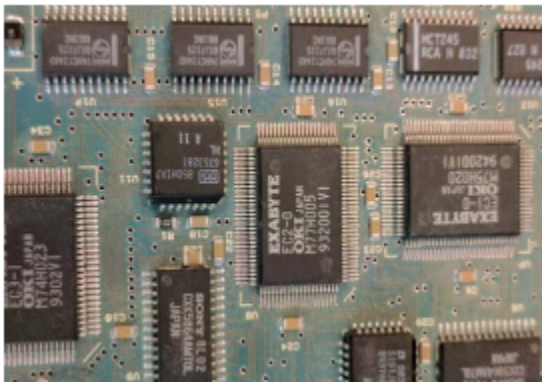

Figure 1. Typical circuit board with surface-mounted integrated circuits or chips.

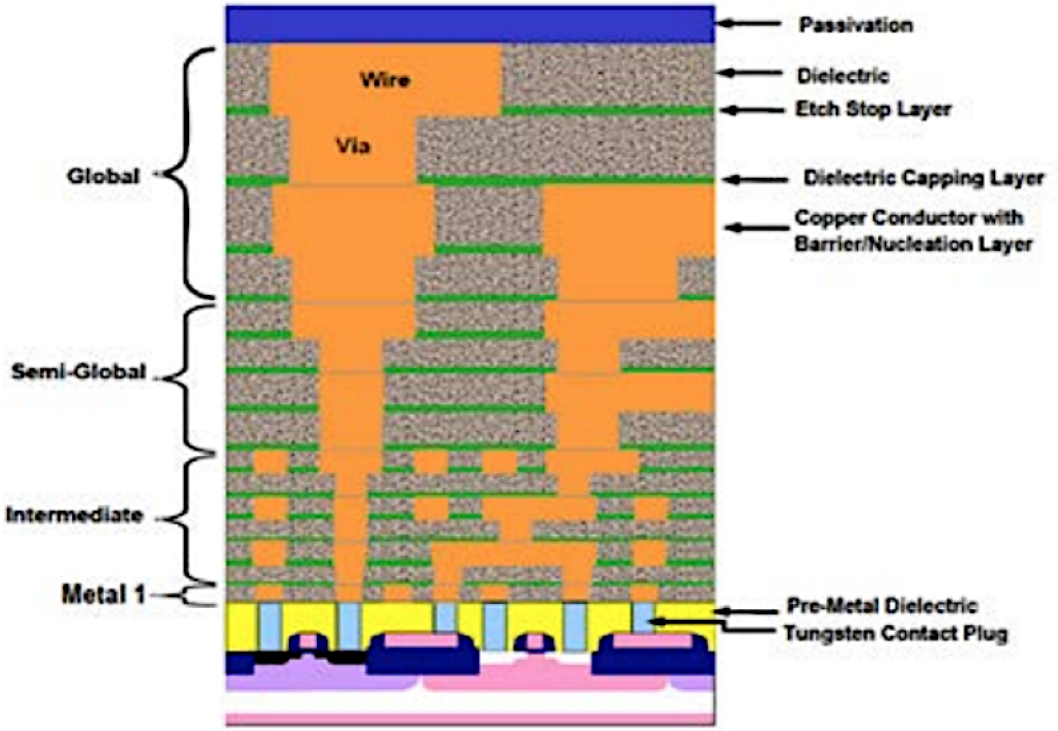

Figure 2. Cross-sectional schematic of an integrated circuit with copper interconnects (orange) [7].

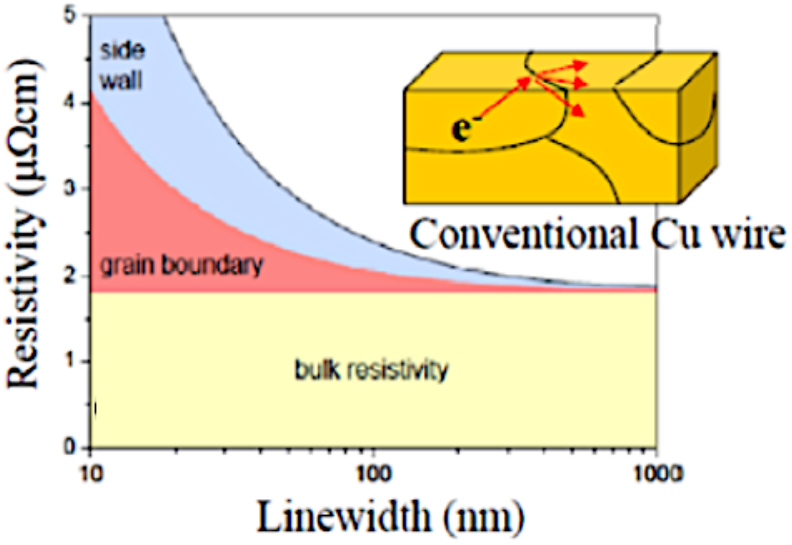

Figure 3. Effect of decreasing linewidth on Cu resistivity [4].

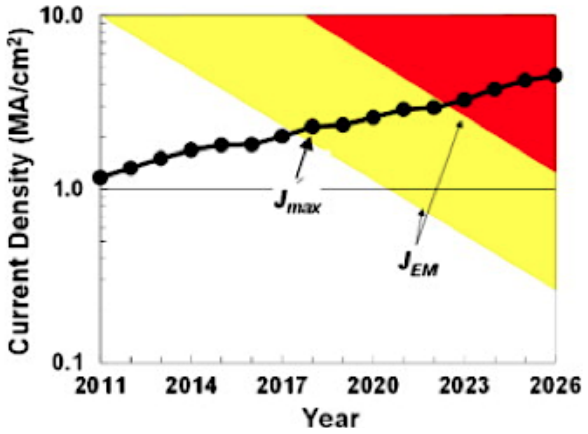

Figure 4. Existing and projected current density requirements for Cu interconnects [4].

1.2 Properties of Nanocarbons

To mitigate the challenges faced by current interconnect materials, our group at SCU has been studying nanocarbon materials as potential replacements, in particular, carbon nanotubes (CNTs) and multi-layer graphene (MLG), as shown in Figures 5 and 6, respectively. CNTs and MLG are among the mechanically strongest materials discovered, in addition to having superior electrical and thermal properties compared to all conventional metals. Furthermore, they are electromigration-resistant [8-10]. Thus, CNTs and MLG are viable replacements for Cu and W in on-chip interconnects.

Existing measurements of nanocarbons indicate current-carrying capabilities to be at least an order of magnitude higher than that of bulk Cu [11]. This means that CNTs and MLG can easily accommodate the projected J_{max} for future generations of IC technology. Since CNTs are made up of rolled up concentric cylinders of graphene sheets, with sp^2-hybridized C-C bonding within the honeycomb structure, CNTs and graphene are both able to create a strong and

conductive structure across the graphitic layer, with excellent electrical and thermal transport. The strong bonding between atoms in CNTs and MLG indicate that these materials will be able to withstand high temperatures as well as electrical and mechanical stresses. This sp^2 C-C-bonding is what makes CNTs resistant to electromigration [12].

While these nanocarbons with excellent properties are viable candidates for future-generation chip technology, many challenges remain in realizing such applications. One major challenge is contact resistance at the interface between nanocarbon and conventional metal, which is unavoidable in integrating it into the chip manufacturing process. Contact resistance results from any heterogeneous interface and has the potential to be the dominate resistance component in any nanocarbon-based structure [13]. If one can take advantage of the sp^2 bonding that both CNTs and MLG possess and form a structure with a continuation of such bonding across the CNT-graphene interface, then the contact resistance of the fabricated test structure can be reduced drastically [14]. This is the motivation for designing a process to fabricate a conductive CNT/MLG structure in our study.

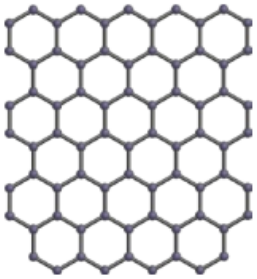

Figure 5. A single layer of graphene with the honeycomb crystal structure.

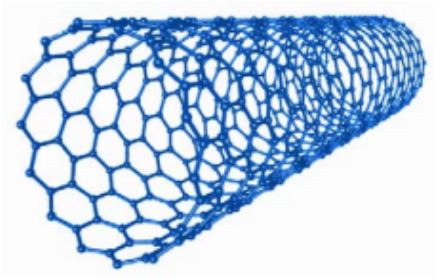

Figure 6. Single-walled carbon nanotube.

Chapter 2: Objectives

2.1 Project Goals

While CNT and Gr are one-dimensional and two-dimensional conductors, respectively, a 3D structure combining the two could potentially form a building block for an on-chip interconnect network and be a viable candidate to replace Cu and W [15]. To create this structure, we aim to (i) design a process for CNT growth on graphene with vertically aligned CNTs and little or no damage to the graphene, (ii) characterize the effect of plasma on CNT alignment in plasma-enhanced chemical vapor deposition (PECVD) reactor, and (iii) measure electrical properties of CNT/MLG test structures to assess the designed process.

2.2 Project Requirements

Based on previous experiments carried out by our research group on CNT growth with various underlayers including Gr and the results obtained [16,17], we embark on the task of designing a process to fabricate CNT/MLG test devices using PECVD, while aiming for a conducting structure with vertically aligned CNT on an undamaged Gr underlayer. Our research group previously determined that growing CNTs using thermal CVD process yields a conductive test structure but results in no alignment, while PECVD growth process yields vertically aligned CNTs but damages the graphene underlayer rendering the sample nonconductive [16]. Thus, the project requirements are to (i) perform CNT growth experiments using various plasma conditions in a PECVD reactor and characterize the fabricated structures using SEM, (ii) measure electrical properties of the created CNT/MLG test structures to assess the design process using a wafer probe station and parameter analyzer, and (iii) vary the process conditions to achieve CNT vertical alignment, prevent damage to Gr, and optimize test structure resistance to a few kΩ or less.

Chapter 3: Experimental Methods

3.1 Growth Process

Based on previous studies from our group [16], there are two possible approaches. One is to adjust the CNT growth conditions using thermal CVD to improve the CNT alignment. Alternatively, the PECVD growth conditions can be varied to lessen the damage to the graphene underlayer while preserving the CNT alignment. Since the CNT alignment is critical for interconnect applications and is a result of the DC electrical field generated by the plasma in the PECVD process, we choose to adjust the strength of this electric field to minimize the damage to the MLG while preserving the CNT alignment.

For the catalyst used in CNT growth, we can use Ni or Co as both have proven to be effective and are compatible with IC manufacturing processes. Ni has been used more extensively as a catalyst for CNT growth than Co, hence there is more information available on using Ni to optimize the growth. On the other hand, Co is currently used in the most advanced IC technology nodes as a replacement for Cu, and CNT growth with Co catalyst results in similar characteristics. The growth results using Co and Ni on a chromium (Cr) underlayer are compared in Figure 7. Using a Co catalyst results in more clustered and less uniform CNTs compared to those using Ni. Thus, the subsequent experiments are all based on CNT growth with Ni catalyst.

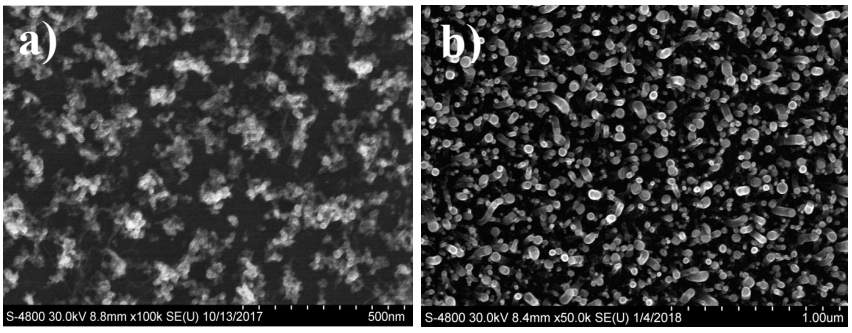

Figure 7. (a) Top-view SEM image of PECVD grown CNT/Cr using Co catalyst. (b) Top-view SEM image of PECVD grown CNT/Cr using Ni catalyst

The fabrication process utilizes a multi-layer graphene on an oxide-covered Si wafer as the substrate. A Ni film, approximately 5 nm thick, is then deposited using a magnetron sputtering system. The sample is then transferred to the CVD reactor, where a PECVD or thermal CVD process is carried out. While both processes are rooted in the generic vapor-liquid-solid (VLS) method for producing nanowires, as illustrated in Figure 8, the PECVD technique includes a plasma step that is not present in the generic VLS method. Unlike PECVD, thermal CVD does not involve the generation of plasma during the CNT growth process. The fabrication processes were described in detail elsewhere [16] and are summarized below.

For both thermal CVD and PECVD, we start by heating the sample in order to dewet the catalyst film into discrete nanoparticles, which are the growth sites for the CNTs. This is followed by flowing ammonia (NH_3) and acetylene (C_2H_2) through the chamber. The dissociated carbon atoms in the acetylene form a CNT on the surface of each catalyst nanoparticle where the growth continues with the nanoparticle remaining at the CNT tip. This process is known as tip-growth. The plasma and DC field in the PECVD process serve to align the CNTs throughout the growth. We observe that the lack of DC electric field in the thermal CVD growth process produces CNTs that have little or no vertical alignment. Once this process is complete, we obtain a sample with CNTs grown directly on MLG. An image of a plasma reactor chamber is shown in Figure 9.

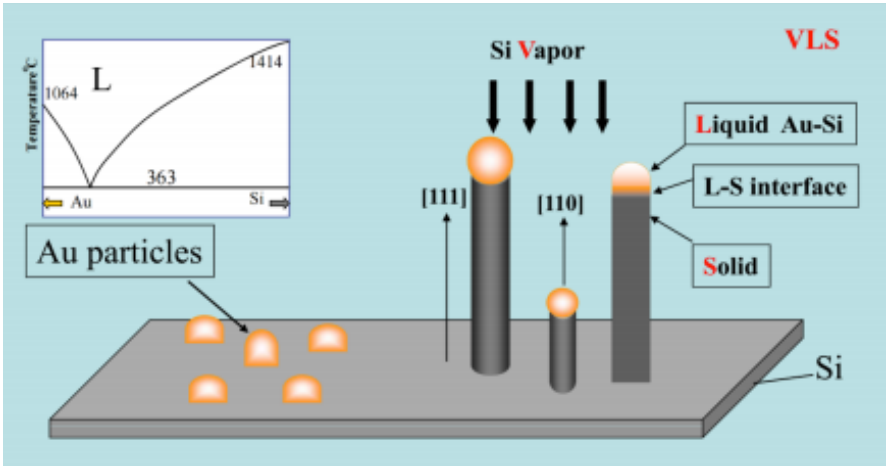

Figure 8. Generic VLS method for producing nanowires. In this schematic, gold nanoparticles are used to catalyze silicon nanowire growth. This process is similar to CNT growth using catalyst film [16].

Figure 9. PECVD chamber during CNT growth. The orange glow is from the heater used to dewet the catalyst film to form nanoparticles. The purple haze is the plasma from gaseous species used for CNT growth. The red arrow points to the substrate where growth occurs [16].

3.2 Process Characterization

We fabricate the CNT/MLG test devices in the Center for Nanostructures' TENT Laboratory located at the NASA Ames Research Center. They are then brought to the EC100 Lab of the Center for Nanostructures for SEM imaging. These images are used to analyze the growth characteristics of each sample such as the CNT diameter, height, and areal density. The wafer probe station in EC100 is used to measure the current-voltage (I-V) characteristics of each sample, from which the total resistance of the CNT/MLG structure can be determined and the contact resistance between the CNTs and MLG underlayer can be extracted.

3.3 Bill of Materials

The materials required for this project are all provided by the TENT Laboratory and listed as follows.

- Silicon wafers with graphene layers
- Growth catalyst sputtering targets
- Methane gas
- Ammonia gas
- Acetylene gas
- PECVD reactor

The majority of the materials required for the process are for sample fabrications. In addition, we are given access to use the SEM and wafer probe station in the Center for nanostructures' EC100 Lab for our sample analyses.

Chapter 4: Results and Discussion

For our project, we fabricate and analyze a large number of samples. While not every sample yields the desirable result, they all nonetheless provide useful information to meet our objectives. The first fabricated test sample consists of CNTs on a Cr underlayer using Ni catalyst and 800 VDC PECVD. This experiment provides a baseline growth recipe and it ensures that all tools are functioning properly. Figures 10(a) and 10(b) show the top and side-view images of the sample

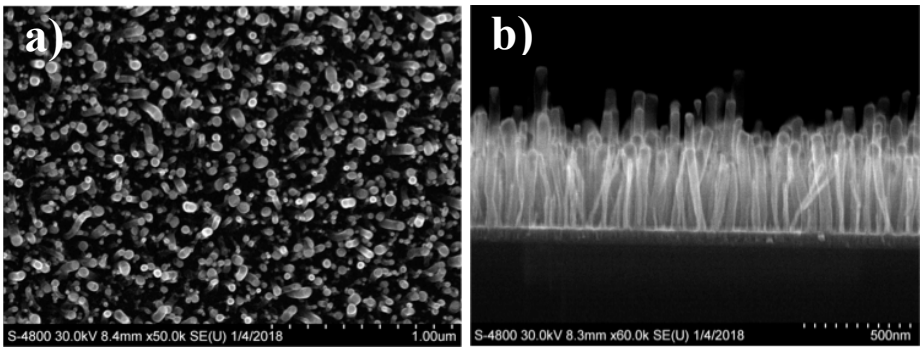

Figure 10. (a) Top-view SEM image of PECVD-grown CNT/Cr. (b) Side-view SEM image of the same sample.

From the top-view image, we obtain a CNT areal density of ~10^{10}/cm^2 and an average CNT diameter of ~55 nm while the side view shows that they are vertically aligned. These results are similar to those obtained previously using the same recipe. They confirm that the reactor is working properly and that we can image the samples effectively using the SEM. The electrical properties of the sample are obtained using the wafer probe station, as illustrated schematically in Figure 11. The results are shown in Figure 12.

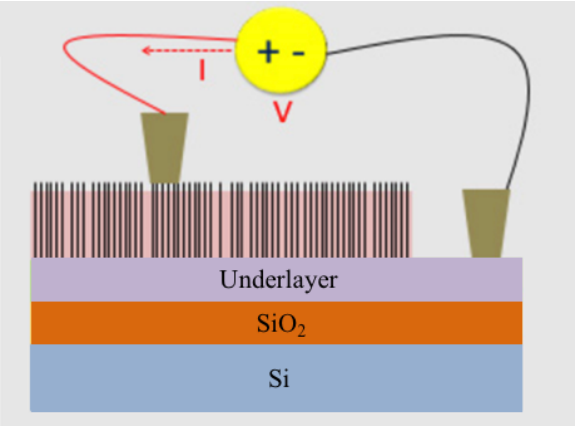

Figure 11. Electrical measurement schematic for probing CNT/Cr test structures [16].

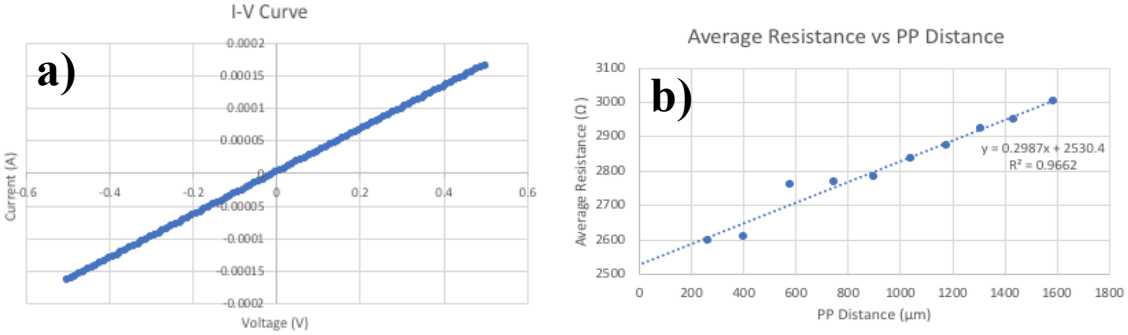

Figure 12. (a) Typical I-V plot between probes on two areas of the CNT/Cr sample. (b) Average resistance versus probe-to-probe (PP) distance plot for the same sample

The linear I-V behavior confirms that the overall conduction is ohmic. The resistance versus PP distance plot infers that electron transports through CNTs and Cr are also ohmic throughout the sample. Each resistance value represents the average from the I-V measurement for that PP distance. Again, this is consistent with past data collected using this recipe.

Before growing CNTs directly on graphene, we need to characterize the plain pre-growth MLG using the SEM and wafer probe station. Based on an estimation of its thickness and the knowledge of graphite interplanar spacing, the side-view SEM image shown in Figure 13(a) confirms that the MLG is uniform and consists of approximately ten graphene layers. The average resistance versus PP distance data shown in Figure 13(b) illustrates the measurement set-up and confirms that the MLG is conductive before the growth and provides us with a baseline for what conductivity to expect from a completely undamaged graphene sample. Furthermore, the contact resistance between the probes and the graphene can be extrapolated from the linear regression of the data points.

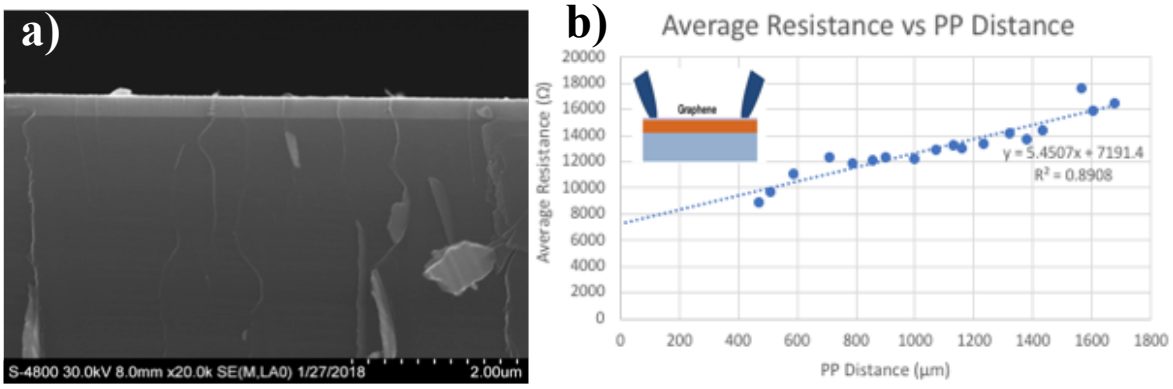

Figure 13. (a) Side-view SEM image of plain MLG on SiO_2. (b) Average resistance vs PP distance for MLG, with the schematic for electrical probing shown in the inset.

From the resistance intercept in Figure 13(b), the contact resistance is extracted to be 7.2 kΩ. If we assume that this contact resistance is due only to the interfaces between each probe and MLG and the two probe contacts are identical, each probe-MLG contact resistance is 3.6 kΩ. We will use this value as a reference for all subsequent data analyses.

We fabricate our first CNT/MLG test sample with Ni catalyst using 800VDC PECVD in order to confirm results obtained previously [16]. Figure 14 shows the top and side-view SEM images of the fabricated sample.

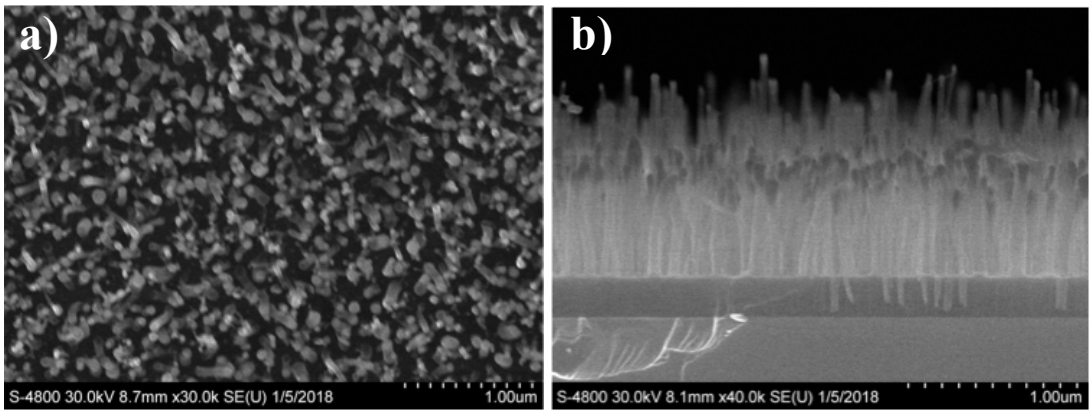

Figure 14. (a) Top-view SEM image of 800VDC PECVD-grown CNT/MLG. (b) Side-view SEM image of the same sample.

From the side-view image, the CNTs are well aligned, and the top-view image reveals a CNT areal density of ~10^{10} /cm^2 is and average diameter of ~65 nm. However, electrical measurements on the sample, as shown schematically in Figure 11 (where the underlayer is now MLG), reveal an open circuit. This is attributed to the damage to the MLG underlayer by the plasma. This result confirms results obtained previously [16].

Next, we set out to demonstrate that by varying the growth process, it is possible to keep the MLG underlayer intact after CNT growth. Thus, we grow CNTs on MLG with Ni catalyst using thermal CVD instead of PECVD. The thermal CVD process does not require creating plasma in the reactor chamber, which could result in little or no damage to the MLG. Figure 15 show the top and side-view SEM images.

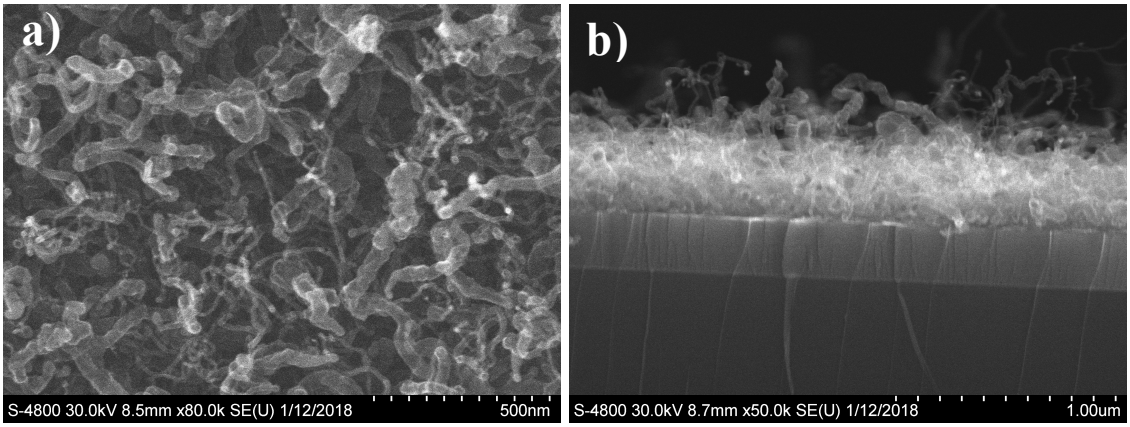

Figure 15. (a) Top-view SEM image of thermal CVD-grown CNT/MLG. (b) Side-view SEM image of the same sample.

Due to the absence of a DC electric field that helps create the plasma in PECVD, the side-view image shows that the CNTs are not aligned at all. However, the electrical measurement results shown in Figure 16 reveal that the sample remains conductive. This finding is also consistent with that obtained previously [16]. The total contact resistance extracted from Figure 16 is 4.4 kΩ, which represents the sum of the probe-CNTs contact (bias probe) and probe-MLG

contact (ground probe). Assuming the probe-MLG contact is similar to that obtained from the plain MLG measurements, the bias probe contact resistance is only (4.4 - 3.6) = 0.8 kΩ. This low value is likely due to residual Ni catalyst film remaining on the sample surface that add a conduction path lowering the resistivity of the sample. From the linear fits to the resistance plots and estimations of probe widths and MLG thickness [17], we find the resistivity of the plain MLG to be 2.1×10^{-5} Ω-cm and that of the thermal CVD-grown sample to be 6.1×10^{-6} Ω-cm. Since the bulk Ni resistivity is 6.9×10^{-6} Ω-cm, the latter result is consistent with the presence of residual Ni film on MLG during thermal CVD.

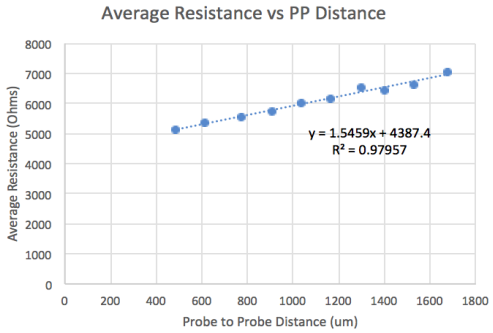

Figure 16. Average resistance vs PP distance for CNTs grown on MLG with Ni catalyst using thermal CVD.

In order to improve the CNT alignment while keeping the MLG undamaged, we set out to experiment with the plasma creation conditions. One series of experiments involves pulsing the voltage to create the plasma at the start of the growth, and another lowers the DC voltage in PECVD. From these experiments, we find that at 500VDC the plasma does not seem to destroy the MLG underlayer since the sample remains conductive. This is important because it shows that we can grow samples using a DC electric field to create plasma and align the CNTs while not damaging the MLG. Therefore, we decide to carry out a detailed analysis of a 500VDC PECVD sample.

Chapter 5: Final Design

The sample consists of CNTs grown on MLG with Ni catalyst using a 500VDC PECVD process. We first obtain SEM images of the sample to ensure there is growth and to study the SEM images and electrical characteristics. The top-view image in Figure 17(a) reveals a CNT areal density of ~10^{10} /cm^2 and average diameter of ~50 nm. Figure 17(b) show improved CNT alignment over that obtained from thermal CVD growth shown in Figure 15, but not as vertically aligned as the 800VDC PECVD sample shown in Figure 14.

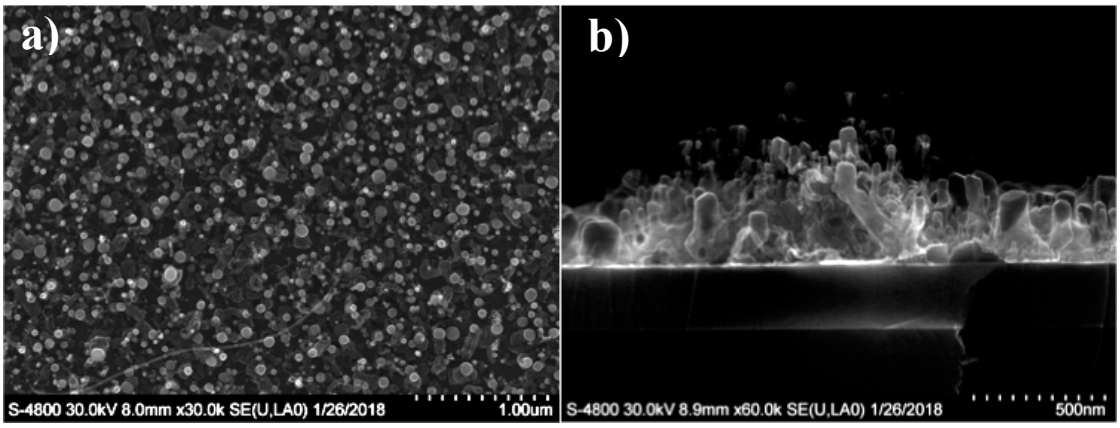

Figure 17. (a) Top-view SEM image of 500VDC PECVD-grown CNT/MLG. (b) Side-view SEM image of the same sample.

The electrical measurement results obtained using the same set-up as in Figure 11 are shown in Figure 18 and confirm that the sample is conductive despite the presence of plasma, with an extracted total contact resistance of 13.5 kΩ. Again, assuming the probe-MLG contact is similar to that obtained from the plain MLG measurements, the bias probe contact resistance is 9.9 kΩ. This is much higher than that found for the sample grown using thermal CVD (0.8 kΩ) and also higher than the probe-MLG contact resistance (3.6 kΩ) for plain MLG. Since the bias probe contact resistance in CNT/MLG consists of probe-CNTs contact, CNTs, and CNT/MLG contact resistances, it is not surprising that its value is as high. To investigate this further, we proceed to estimate the MLG resistivities from the resistance versus PP distance plots for the plain MLG and this CNT/MLG sample.

Again, from the linear fits, probe widths, and MLG thickness, the extracted MLG resistivities are 2.1×10^{-5} Ω-cm for plain MLG, and 3.5×10^{-5} Ω-cm for the CNT/MLG sample grown using 500VDC PECVD. Both values are about an order of magnitude higher than that of a graphene sheet [18]. The closeness of these two MLG resistivities, together with the extracted contact resistances suggests that the conduction path in either case traverses the MLG as well as the CNTs in the latter. But in the case of the CNT/MLG sample, the graphene has undergone a plasma growth process to grow the CNTs and has likely sustained some damage, albeit remaining conductive. Nevertheless, the results confirm that the growth process causes little or no damage to the MLG.

To examine further the bias probe contact in measuring CNT/MLG resistance, we perform I-V measurements on the CNT/MLG sample with a nanoprober and obtain some preliminary results, as shown in Figure 19, which also contains results obtained using the wafer probe station for comparison. The extracted contact resistance is 32 kΩ, which is expected as the nanoprobe tip is much smaller than that of the wafer probe. The extracted graphene resistivity is 5.7×10^{-4} Ω-cm, significantly lower than the other extracted values. However, these results are very preliminary and more detailed study is needed to determine the contact resistance and MLG resistivity reliably using the nanoprober.

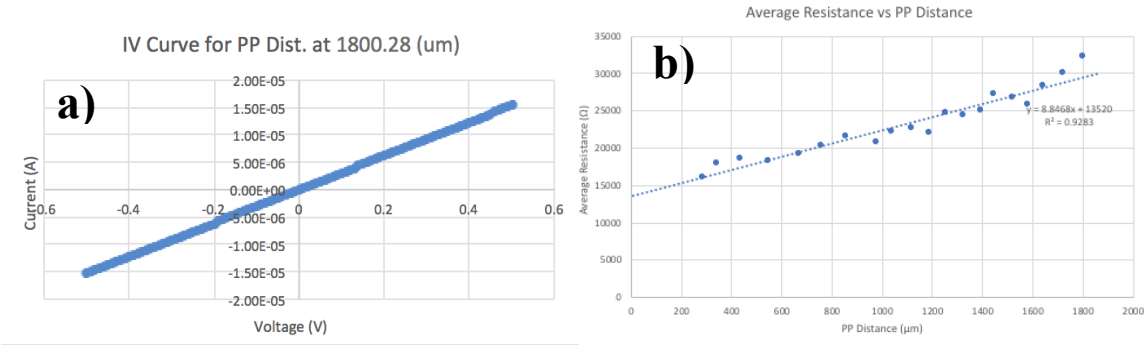

Figure 18. (a) I-V Curve of one point on CNT/MLG sample grown using 500VDC PECVD. (b) Average resistance vs PP distance for the sample.

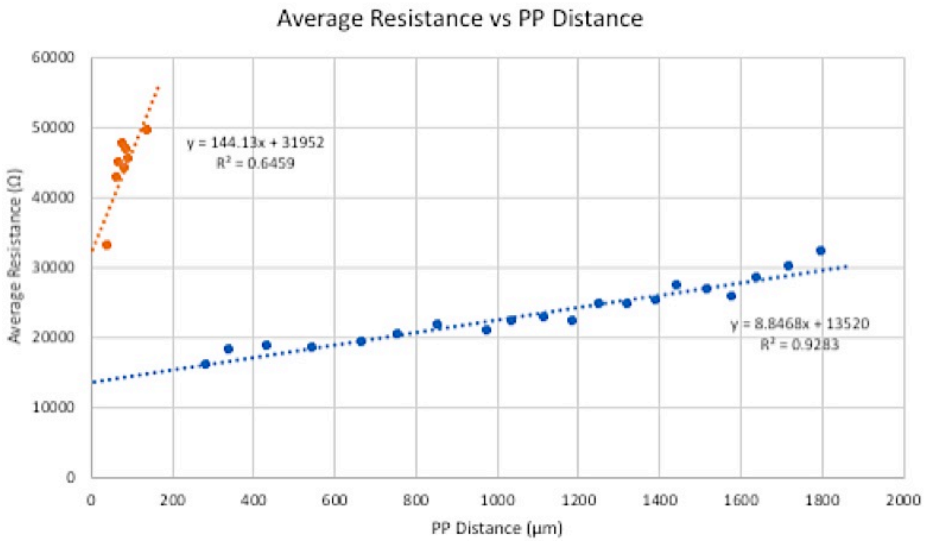

Figure 19. Comparison of average resistance (R) vs PP distance for CNT/MLG sample using wafer probe station (blue) and nanoprober (orange).

Chapter 6: Professional Issues and Constraints

6.1 Economic Implications

We analyze the economic impact of our project by observing the effects of Moore's law and the continuing improvement of integrated circuits. The improvements in chip performance allow for faster devices with more computing power. These improvements allow for more useful functions to be installed on these devices, that would otherwise have limited capabilities due to limitations of the hardware. A good example of this is big data processing. Building a system to analyze large amounts of data requires a significant amount of processing power resulting in a need for chips to be faster, smaller, and more efficient. As this processing power increases these big data processing systems can improve and analyze a larger quantity of data. Furthermore, the research into CNT-graphene interconnects can allow for advancement in many other fields. Our project can potentially lead to improvements in chip performance and reliability. If implemented

in integrated circuits, CNT and Gr could result in chips that are faster and last longer. However, the cost for such implementation is difficult to estimate at this time.

6.2 Health, Safety, and Environmental Impact

In order to evaluate the environmental impact of the CNT/Gr fabrication, we analyze the environmental impact of the individual materials used during the manufacturing process. Argon, which is used during both the sputtering and growth process, is a naturally occurring element in the environment. The gas rapidly dissipates in well-ventilated areas and has no adverse environmental consequences [19]. Further, argon is not ozone depleting, which means that using argon does not contribute to global warming [19]. Nitrogen gas flows through the sputtering machine to help depressurize the chamber without oxidizing the sample. Nitrogen is a naturally occurring element that makes up approximately 78% of the Earth's atmosphere [15]. Various nitrogen compounds, such as nitrogen oxide (N_2O), have adverse effects on the environment. When N_2O dissolves in atmospheric water it produces acid rain which is corrosive to stone and metal work [20]. Furthermore, nitrogen oxides contribute to the destruction of the ozone layer. Fortunately, the sputtering process uses nitrogen gas (N_2) which is inert, and the process does not result in any reaction involving nitrogen.

The use of ammonia gas involves a significant carbon footprint. The production of ammonia (NH_3) produces a fair amount of CO_2. In 2010, the global CO_2 emissions from ammonia production was around 450 million metric tons. That means that the "global average is around 2.867 tons of CO_2 emitted per ton of NH_3 produced" [21]. Lastly, pure acetylene is relatively nontoxic and poses no environmental hazard as an air pollutant [22]. If CNTs become integrated into the IC industry, then the environmental effects would need to be evaluated, but due to the small amount of ammonia used in our project, the environmental impact is minimal.

Caution must be taken when disposing of CNT samples because CNTs can be harmful if ingested. Therefore, it is important to take the necessary precautions for hazardous material disposal to avoid possible food and water contamination. Alternatively, there are many companies that recycle wafers. Companies can reclaim wafers by reconditioning the surface of an already processed wafer. While disposal of our samples must conform to environmental safety regulations, the graphene substrate can be recycled rather than disposed of. Throughout our project proper safety protocols are followed.

Chapter 7: Conclusions and Future Work

7.1 Summary and Conclusions

Our experiments confirm the findings of previous work from our group [16]: That using PECVD at 800VDC to grow CNTs on MLG results in vertically aligned CNTs while damaging or destroying the MLG underlayer. We also confirm that using thermal CVD (no plasma) results in a conductive structure but CNTs are not aligned. After extensive experimentation and analyses, we find that the graphene remains intact in CNT/MLG structures fabricated using 500VDC PECVD, with improved CNT alignment over that obtained with thermal CVD. Electrical probing of resulting CNT/MLG structures confirms conduction, although the challenge remains in making better nanoprobe contact with only CNTs in order to determine CNT/MLG contact resistance.

7.2 Future Work

More work on the fabrication process is needed to improve CNT alignment and increase areal density using PECVD so that the resulting sample can be properly probed. Such improvement would facilitate the extraction of CNT/MLG contact resistance, which is critical to optimizing the contact through continuation of sp^2 C-C bonding across the interface. When this is achieved, the 3D all-carbon CNT/MLG nanostructure will be a viable building block for interconnects in the most advanced IC technology node.

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Appendix A: Senior Design Conference Slides as Presented

Process Optimization for Carbon Nanotubes-on-Graphene Fabrication

Andrew Michelmore and Julia Shaffer

Advisor: Dr. Cary Y. Yang

1

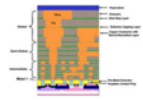
Outline

- Background
- Project Objectives
- Project Requirements
- Block Diagram
- Test Structures and Results
- Conclusions
- References
- Acknowledgements

2

What is in an Integrated Circuit?

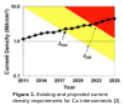
- **Components**: transistors, diodes, capacitors, resistors
- **Interconnects** or wires linking components to perform designed functions



3

Introduction

- Challenges in sub-20nm integrated circuit or chip technology
  - Performance and reliability problems due to existing interconnect materials, Cu and W
- Reduction in interconnect linewidth
  - Resistivity increases with reduced linewidth
  - Current density exceeding metal current capacity, resulting in electromigration
- Nanocarbons as potential replacement for Cu and W [3]
  - Electromigration-resistant
  - Low electrical resistance
  - High thermal conductivity

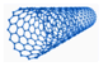


4

Nanocarbons

- Graphene is a 2D material made entirely of carbon atoms in a honeycomb structure.
- A Carbon Nanotube is a structure formed by rolling graphene sheets into one or multiple concentric cylinders.

Graphene

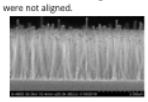


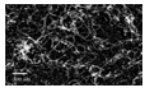
CNT

5

Background

- Our group previously found that CNTs grown directly on multi-layer graphene (MLG) using plasma-enhanced chemical vapor deposition (PECVD) yielded vertically aligned CNTs but the structure was non-conducting due to damages in MLG underlayer.
- We also found that using thermal CVD (without plasma) kept MLG intact, but CNTs were not aligned.





6

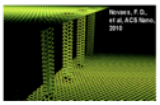
Project Objectives

- Achieve a 3D all-carbon conducting structure that serves as the building block for on-chip interconnect networks [5].
- Design a process for CNT growth on MLG with vertically aligned CNTs and little or no damage to MLG [6].
- Perform CNT growth experiments using various conditions to create plasma in PECVD reactor and characterize the fabricated structures using scanning electron microscopy (SEM).
- Measure electrical properties of CNT/MLG test structures to assess designed process, using wafer probe station and parameter analyzer as well as *in situ* nanoprobing in SEM [7].

7

Project Requirements

- 3D conductive all-carbon nanostructure consisting of vertically aligned CNTs on horizontal MLG, with resistance of a few kΩ or less.
- Undamaged MLG after CNT growth.
- CNT growth using lower DC plasma voltage in reactor (currently 800 V).



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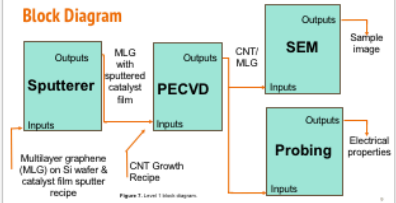
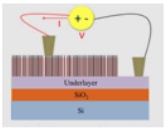
Block Diagram



9

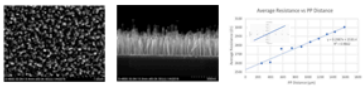
Setup for Resistance Measurements

- Ground probe fixed on underlayer while bias probe is lowered to ensure direct contact with CNTs.



10

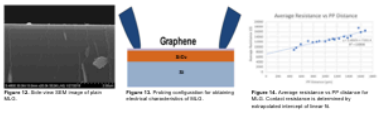
CNTs grown on Cr with Ni Catalyst using 800VDC PECVD



- Experiment to test baseline growth recipe and to ensure proper functioning of equipment.
- Linear I-V behavior and resistance versus probe-probe distance plot confirm ohmic conduction.

11

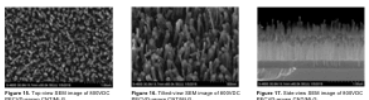
Plain Graphene



- The extracted contact resistance of about 7 kΩ consists of mostly probe-MLG resistance. This result will be used for analyzing all subsequently fabricated CNT/MLG samples.

12

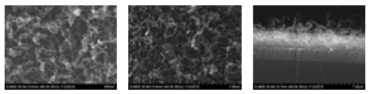
CNTs grown on MLG with Ni catalyst using 800VDC PECVD



- CNTs grown using the same recipe as that on Cr underlayer to confirm viability of direct CNT growth on MLG.
- The SEM images show that the CNTs are vertically aligned.
- The structure is not conductive due to plasma damage to MLG underlayer.

13

CNTs grown on MLG with Ni catalyst using Thermal CVD

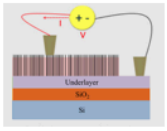


- CNTs grown on MLG using thermal CVD process (no plasma).
- Sample is conductive but CNTs not aligned.

14

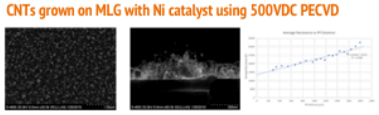
Setup for CNT/MLG Resistance Measurements

- Ground probe fixed on graphene while bias probe lowered at small increments to ensure direct contact with CNTs.
- Nanoprobing enhances the probability of making direct contact with CNTs.



15

CNTs grown on MLG with Ni catalyst using 500VDC PECVD



- I-V and resistance results show conduction with higher overall resistance than that of plain MLG, with bias probe probably making direct contact with graphene.
- CNTs not as well aligned as those obtained using 800VDC, but improved alignment over those with thermal CVD.
- Reduced DC voltage in PECVD appears to preserve MLG underlayer.

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CNTs grown on MLG with Ni catalyst using 500VDC PECVD

- Nanoprober results confirm conduction in CNT/MLG structure, with higher resistance attributed to narrower probe tips than those in wafer probe station.
- Difference in slopes of R vs d plots suggests probable conduction through CNTs as well as graphene.

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Summary of Experimental Challenges

- Improve CNT alignment and areal density to facilitate nanoprobing and reduce resistance.
- Develop a technique to ensure nanoprobe making contact with CNTs only, so that CNT/MLG contact resistance can be extracted.

18

Conclusions

- Our experiments confirm the findings of previous work from our group [4], showing that using PECVD at 800VDC to grow CNTs on MLG results in vertically aligned CNTs, while damaging or destroying the MLG underlayer. We also confirm that using thermal CVD (no plasma) results in a conductive structure but CNTs are not aligned.
- CNT/MLG structures fabricated using 500VDC PECVD reveal that graphene is intact with improved CNT alignment over that from thermal CVD.
- Electrical probing of resulting CNT/MLG structures showed conduction, though challenge remains in making nanoprobe contact only CNTs in order to determine CNT/MLG contact resistance

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References

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- Dayou Luo, SCU
- Dr. Ben Lee
- Dr. Jessica Koehne, NASA Ames
- Shaun Snyder, SCU
- Dr. Cary Yang, SCU

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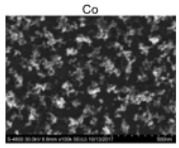
Thank You!

22

Additional Prepared Slides (Not Presented):

Different Catalysts

Co



Ni

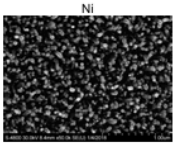


Figure 33. Top-View SEM image of PECVD grown CNT/Cr using Co catalyst

Figure 34. Top-View SEM image of PECVD grown CNT/Cr using Ni catalyst

25

Health and Safety

- Research on health effects of CNTs suggested that if released into air they could potentially be inhaled [9].
- Additional research needed to study the health effects of CNTs.

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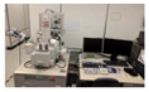
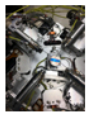
Analysis Equipment





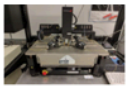


Figure 26. Scanning Electron Microscope

Figure 27. Nanoprobers

Figure 28. Wafer Probe Station

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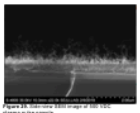
Additional Experiments

- Pulsed plasma growths
  - This is to analyze whether the damage from plasma is being done at the beginning of the growth process or if it is due to a prolonged exposure to plasma



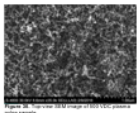


Figure 31. Top-view SEM image of 800 VDC plasma pulse sample.

Figure 30. Top-view SEM image of 800 VDC plasma pulse sample.

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Additional Nanoprobing Results

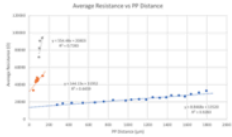

Figure 25. Comparison of average resistance (R) vs PP distance (d) for CNT/MLG sample using wafer probe station (blue), nanoprober (orange), with the CNT conduction path (gray).

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Probe Marks

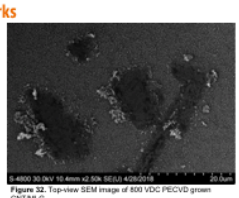

Figure 32. Top-view SEM image of 800 VDC PECVD grown CNT/MLG.

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Appendix B: Information on Equipment used for Project

Detailed information on the construction and use of our Hitachi S-4800 scanning electron microscope is available at the following URL:
https://cmrf.research.uiowa.edu/sites/cmrf.research.uiowa.edu/files/Hitachi%20S-4800%20User%20Instructions.pdf

Detailed information on the construction and use of our Cascade Microtech wafer probe station is available at the following URL:
https://www3.nd.edu/~nano/facilities/at_man_Cascade12000SemiAutoProbe_Nucleus_Manual.pdf

Detailed information on the construction and use of our Zyvex S200 nanoprober is available at the following URL:
http://www/zyvex.com/Documents/S200.pdf

Appendix C: Project Presentations and Publication

1) D. Luo, R. Senegor, J. Shaffer, A. Michelmore, C. Y. Yang, "Fabrication of 3D Nanocarbon Structure for Potential Sensor Applications," Poster presentation at the 233rd Electrochemical Society Meeting, Seattle, Washington, May 13-17, 2018.

2) J. Shaffer, A. Michelmore, R. Senegor, D. Luo, C. Y. Yang, "Process Optimization for Carbon Nanotubes-on-Graphene Fabrication," Poster presentation at the 46th Annual Northern California Electronic Materials Symposium, Santa Clara, May 4, 2018.

3) A. Michelmore, J. Shaffer, R. Senegor, D. Luo, C. Y. Yang, "Process Optimization for Carbon Nanotubes-on-Graphene Fabrication," Poster presentation at the 2nd Annual Santa Clara University School of Engineering Research Showcase, Santa Clara, February 23, 2018.